SysML Modeling of Power Electronics Converters for Microgrid Applications

Alonso Gutierrez, Corinne Alonso, Fernando Jiménez

SysML Modeling of Power Electronics Converters for Microgrid Applications

Alonso Gutiérrez Galeano[1-2], Corinne Alonso[1], Fernando Jiménez[2]
[1]LAAS-CNRS
7, avenue du Colonel Roche
BP 54200 31031 Toulouse cedex 4, France
[2]Universidad de los Andes
Cra 1 Nº 18A- 12
111711 Bogotá, Colombia

E-mail : agutierr@laas.fr

Abstract

Currently, power electronics converters in microgrids have increased their application and complexity; as a result, innovative design methodologies are required. Hardware-in-the-Loop real-time emulations arise as an interesting modeling alternative to study the behavior of power converters for demanding conditions such as the integration to microgrids. This work presents in detail a method to design and implement in FPGA models of power converters to Hardware-in-the-Loop real-time emulations. These models are described by the Systems Modeling Language (SysML) and the HiLeS formalism. The proposed approach transforms high level model descriptions from SysML diagrams to HiLeS formalism and Petri nets for implementations in FPGA. Finally, the results of these implementations in embedded hardware are compared with conventional methods of simulation.

1. Introduction

Power electronics in microgrids considers numerous applications [1][2] such as power converters to control the power flow of renewable energy resources with the electrical grid. Furthermore, the increased diffusion of microgrids requires higher flexibility and reliability shows new challenges for conventional power electronics systems [3]. As a result, the power electronics growth and the integration of alternative energy resources require more power electronics equipment with high efficiency and flexibility.

In addition, power electronics systems with innovative control strategies are needed to achieve the current requirements of power electronics. However, power electronics in microgrids requires more powerful processing devices because of the increment of its control complexity [4].

These control systems for power electronics in microgrids need high performance devices; as a result, solutions based on FPGA arise as suitable option. However, these control system implementation in FPGA require appropriated schemes to accomplish the control specifications [5]. Therefore, novel methodologies are required to increase the productivity and to decrease the efforts for implementation in hardware.

Taking into account the previous factors, the HiLeS Platform is proposed as a design methodology for Hardware-in-the-Loop simulations based on FPGA of power electronics in microgrids.

The HiLeS platform [6][7] is a tool and methodology intended to generate Petri net representations and VHDL code from SysML models. The HiLeS platform is developed to design and implement complex electronic systems in FPGA. These complex electronic systems include control systems and Hardware-in-the-Loop models represented by SysML diagrams. Moreover, HiLeS characteristic of converting SysML diagrams in Petri nets [8], which allows validating the SysML models from Petri net representations.

In addition, structural validation of SysML models through Petri nets allow to analyze the structural stability previous to implementation in embedded hardware. Therefore, the HiLeS platform is shown in this paper as a suitable tool and methodology to design Hardware-in-the-Loop models of power converters intended to be implemented in FPGA.

2. Hardware-in-the-Loop Simulations in Microgrid

Hardware-in-the-Loop is a technique used to develop real-time emulation systems. The emulation systems provide a suitable environment to evaluate physical and control systems [9].

This technique includes electrical sensors and actuators which act as interface between the simulated system and the embedded control system. Therefore, the sensors are controlled by the simulated signals, and the control algorithms send control signals to the actuators. As a consequence, changes in the control signals produce changes in the simulated system.

These emulations allow the design and implementation of control systems in embedded hardware. In fact, embedded control system could be tested in emulated systems without most of the actual plant limitations. For example, testing a power electronics control as an actual plant could create dangerous conditions for the power device.

Power electronics simulations in microgrids are driven toward Hardware-in-the-Loop tools. This technology allows the design and power electronics test in microgrid systems reducing the validation time, increasing efficiency, and improving reliability of microgrids.

Hardware-in-the-Loop simulations for microgrid systems also are used to verify the stability, operation, and fault tolerance of microgrids [10]. Real-time emulations of microgrids have the capacity to model power systems that includes several components associated to generators, loads, alternative energy sources, and electrical grid interconnections. These types of simulation allow the evaluation and analysis in real-time of microgrid power systems in practical emulated environment. In addition, hardware emulation technique can be used in microgrids to explore the integration of renewable energy resources, and innovative control systems.

3.HiLeS Formalism

Petri net is a formal language which is used to model discrete events systems [11][12]. Petri nets are based on graphical notation to represent sequential and concurrent process. Petri nets are currently used to model and verify designs in different domains. HiLeS (High Level Specification of Embedded Systems) formalism [13][14] consists of a language and a methodology based on Petri nets which incorporates continuous behavior and hierarchy.

The HiLeS formalism is intended to support embedded system design. Furthermore, HiLeS formalism defines the rules to represent a HiLeS model in hardware description languages such as VHDL. These characteristics enable designers to build virtual prototypes allowing technological independence, operational verifications, and formal verification of specifications.

The HiLeS formalism is intended to support the processes of designing formal behavioral models and to integrate features of high level graphic semantic. HiLeS allows describing asynchronous and concurrent behaviors; also, it describes time-driven event or mixed-driven dynamics [15].

4. SysML Modeling

SysML is a graphical language for modeling engineering systems. Diagrams of SysML are *Block Definition Diagrams*, *Internal Block Diagrams*, and *Activity Diagrams*. SysML uses *Block Definition Diagrams* (BDD) to illustrate the structural composition of systems, and *Internal Block Diagrams* (IBD) to describe the relation among the system components. Furthermore, SysML depicts the system behavior by means of *Activity Diagrams* [16].

4.1 From SysML to HiLeS Formalism

The HiLeS platform is intended to generate Petri net representations and VHDL code from SysML models. Fig. 1 shows the SysMLtransformation chain used by the HiLeS platform. In Fig. 1, transformation T1 provides the synthesis from SysML models to HiLeS formalism. T2 is used to produce Petri nets representations from HiLeS models. Additionally, transformation T2 transforms the Petri net in textual format to validate the Petri nets by TIme petri Net Analyser (TINA). Finally, transformation T3 is used to transform HiLeS description in VHDL language.

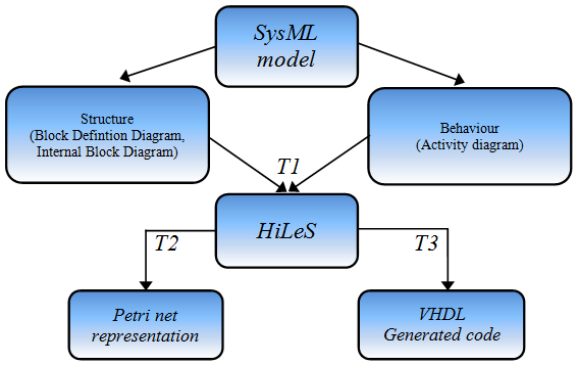

Figure 1. SysML transformation chain in HiLeS-RCP.

The behavior transformation consists of creating the required HiLeS Control Net (HCN) from SysML Activity Diagrams. The main advantages of using Activity Diagrams in SysML models are their direct representation in Petri nets. A detailed description of this transformation is found in [7].

In this approach, there are two types of actions described in Activity Diagrams: Call Behavior Actions and Call Operation Actions. Call Behavior Action are used to describe other Activity Diagrams equivalent to hierarchical construction. As result, Call Behavior Actions creates structural block and adds the required HiLeS Control Net elements to correctly represent the model behavior.

The transformation from SysML models to HiLeS Control Net based on Petri nets allows the automatic

VHDL code generation. Fig. 2 shows the partial synthesis for the VHDL code generated using the HiLeS platform

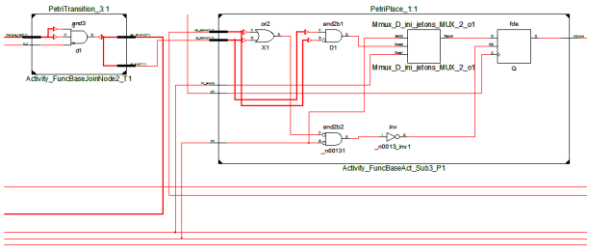

Figure 2. Partial synthesis of VHDL code generated by the HiLeS platform.

5. SysML Model of Boost Converter

Boost converters are power converters of wide application in microgrids. In a boost converter the input voltage is increased; as a consequence, the output voltage is higher than the input voltage [17]. Fig. 3 shows a conventional boost converter circuit including losses associated to inductor (R_L).

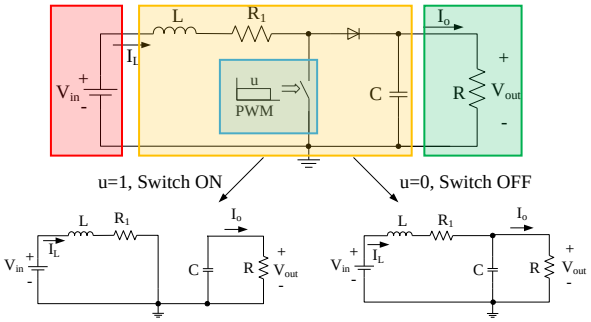

Figure 3. Boost converter.

Fig. 4 shows the flow of operations to describe the behavior of a boost converter according to [18].

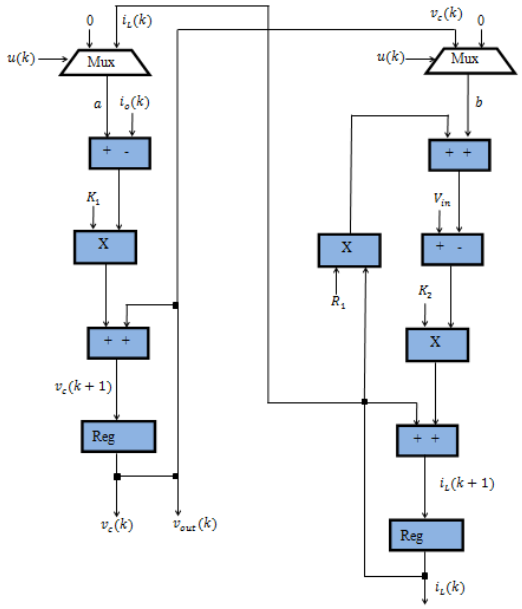

Figure 4. Data flow graph to the boost converter model

The power system for the boost converter modeled using SysML is described in figures 5, 6, and 7.

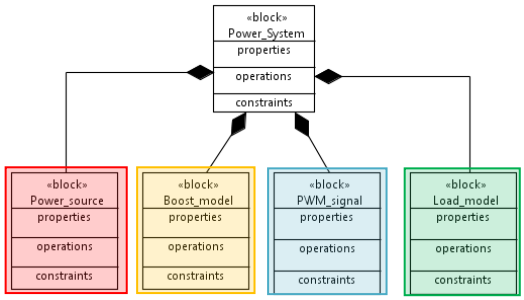

Figure 5. Block Definition Diagram of boost converter model

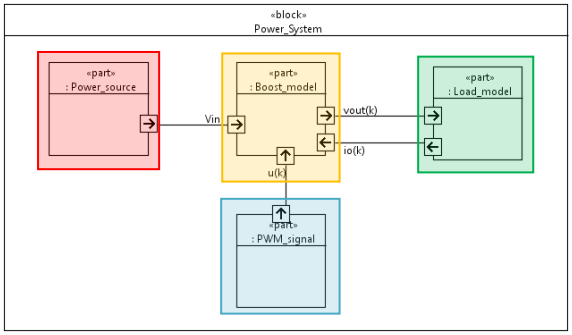

Figure 6. Internal Block Diagram of boost converter model

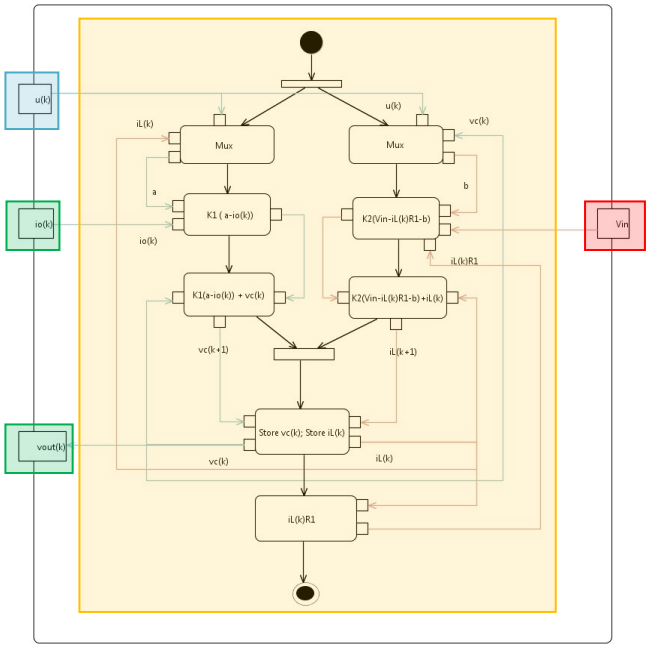

Figure 7. Activity Diagram of boost converter model

The implementation in embedded hardware of the boost converter system modeled by SysML in the HiLeS platform is presented in the following figures. Math operations in FPGA are calculated in float point format with simple precision (IEEE 754 standard).

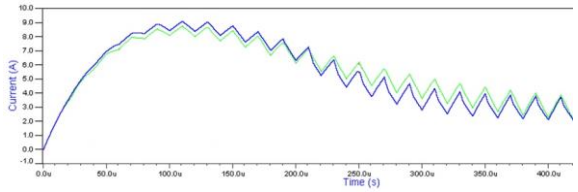

Figure 8. Inductor current of boost converter
(model VHDL – conventional simulation)

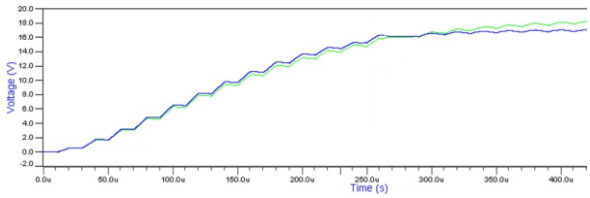

Figure 9. Capacitor voltage of boost converter model in VHDL
(model VHDL – conventional simulation)

6. Conclusions

This study described a progressive and modular methodology to model power converters integrated to microgrids. The proposed approach showed the flexibility to use the HiLeS platform and its performances to represent the global behavior of power converters. This methodology allows the study of power converters and their interaction with other parts of the system. In addition, this approach presents properties of modularity and high degree of scalability. Future work is to develop additional models to study complex microgrids including other converter topologies and control algorithms.

References

[1] S.K. Bhattacharya, Fundamentals of Power Electronics, Vikas Publishing House, New Delhi, pp.11 (2009).

[2] M. Jamil, B. Hussain, M. Abu-Sara, R.J. Boltryk, and S.M. Sharkh, Microgrid Power Electronic Converters: State of the Art and Future Challenges, Universities Power Engineering Conference (UPEC), Glasgow, (2009).

[3] T. Midtsund, Control of Power Electronic Converters in Distributed Power Generation Systems, Master Thesis in Energy and Environment, Norwegian University of Science and Technology, (2010).

[4] E. Monmasson, L. Ahoucine, and M. Ohamed, FPGA-Based Controllers - Different Perspectives of Power Electronics and Drive Applications, IEEE Industrial Electronics Magazine, pp.14-26, (2011).

[5] A. Myaing and V. Dinavahi, FPGA-based real-time emulation of power electronic systems with detailed representation of device characteristics, IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 358–368, (2011).

[6] H. Hoyos, R. Casallas, and F. Jiménez, HiLeS-T: an ADL for Early Requirement Verification of Embedded Systems, in Proceedings of the 5th International Workshop on Model Based Architecting and Construction of Embedded Systems, New York, (2012).

[7] HiLeS project. Universidad de los Andes, Colombia, Available in: https://hiles.uniandes.edu.co/

[8] C. Gomez, P. Esteban, J. Pascal, and F. Jimenez, Modeling complex system using SysML, Report LAAS N 09636, (2009).

[9] C. Yoo, W. Choi, I. Chung, D. Won, S. Hong, and B. Jang, Hardware-in-the-Loop Simulation of DC Microgrid with Multi-Agent System for Emergency Demand Response, IEEE Power and Energy Society General Meeting, San Diego (2012).

[10] Y. Li , D. M. Vilathgamuwa, and P. C. Loh , Design, Analysis, and Real-Time Testing of a Controller for Multibus Microgrid System, IEEE Trans. Power Electron., vol. 19, no. 5, pp.1195 -1204 (2004).

[11] David R., Alla H., Discrete, Continuous, and Hybrid Petri Nets, 2nd Edition, Springer, New York, (2010).

[12] B. Berthomieu , F.Vernadat, Time Petri Nets Analysis with TINA, Third International Conference on Quantitative Evaluation of Systems, pp. 123-124, (2006).

[13] H. Hoyos, R. Casallas, and F. Jiménez, ADL for Early Requirement Verification of Embedded Systems, in 5th International Workshop on Model Based Architecting of Embedded Systems, (2012).

[14] F. Jimenez, Specification et Conception de Micro-Systemes Bases sur des Circuits Asynchrones, PhD thesis, Institute National des Sciences Appliquees (Toulouse, France), Universidad de los Andes (Bogota, Colombia), (2000).

[15] H. Hoyos, F. Jiménez, R. Casallas, D. Correal, Tucan - Virtual Prototype Generation and Time Constraints Analysis of Real-Time Embedded Systems, Design Automation for Embedded Systems, Springer, New York, (2013).

[16] Object Management Group, Systems Modeling Language, SysML, (2010).

[17] R. W. Erickson, Fundamentals of Power Electronics, Chapman and Hall. New York. Second Edition, (1997).

[18] A. Gutierrez, H.R.Chamorro, and J.F. Jimenez, Hydroelectricity and Power Electronics: Environmental Impacts, Emerging Technologies and Challenges. Chapter: Hardware-in-the-Loop Simulations and Control Systems Based on FPGA for Power Electronics in Microgrids. Nova publishers, New York, (2014).