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Mouna Mahane, David Trémouilles, Marise Bafleur, Benjamin Thon, Marianne Diatta, et al.. New triggering-speed-characterization method for diode-triggered SCR using TLP. Microelectronics Reliability, 2017, 76-77, pp.692 - 697. 10.1016/j.microrel.2017.07.063 . hal-01643028

HAL Id: hal-01643028
https://laas.hal.science/hal-01643028

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Microelectronics Reliability xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

New triggering-speed-characterization method for diode-triggered SCR using TLP

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ARTICLE INFO

Article history:
Received 28 May 2017
Received in revised form 12 July 2017
Accepted 14 July 2017
Available online xxxx

Keywords:
Critical charge
DTSCR
Electrostatic discharge (ESD)
IEC
Radio frequency (RF)
TLP
Turn-on time

ABSTRACT

The key parameters in the optimization of the Diode Triggered Silicon-Controlled Rectifier (DTSCR) as a RF ESD protection, are the turn-on time and the trigger-voltage overshoots seen before the SCR turns on, during very fast ESD transients [1]. But at this time, there is no normalized method to evaluate and report the ESD device turn-on speed [2]. Such a method would be required to effectively compare device performance. In this work a new method, based on stored-charge, is investigated to characterize the triggering speed of DTSCR using Transmission Line Pulsing (TLP) measurements.

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1. Introduction

Among various SCR devices, the Diode Triggered Silicon-Controlled Rectifier (DTSCR) prevails as an attractive ESD protection for high frequency circuits [3]. Due to its low capacitance, the DTSCR offers no interference with protected-circuit functionality. Its flexible design parameters allow a tunable trigger voltage. Besides, its low on-resistance and holding voltage lead to a less local power dissipation ($I_{ESD} \times V_h$), which guarantees a high robustness to large number of ESD stress models [4].

But, even if DTSCR exhibits attractive ESD performance, it still has voltage overshoots caused by a slow turn-on time during ESD discharge; especially for CDM ESD stress that presents very short rise time [1].

In this paper, a new method, inspired by the critical charge theory, is investigated to extract the turn-on time of the DTSCR structure. Sections 2 and 3 describe the ESD protection used in this work, and give the global definition of turn-on time for thyristor devices. Section 4 investigates on the existing methods to extract the turn-on time from TLP characterizations. And Section 5 proposes two approaches based on conductance and stored charge to extract the turn-on time from TLP and IEC characterizations. In Section 6, the triggering process of DTSCR is investigated using TCAD simulation. And in Section 7, this new extraction method is used to compare turn-on speed performance of two DTSCR structures.

2. DTSCR structure

Fig. 1 shows a schematic representation of the DTSCR used in this work. It is an ESD protection for RF applications meeting IEC 61000-4-2 Level-4 (8 kV), with ultra-Low capacitance, down to 0.5 pF.

During a positive ESD event at the Anode, the *TVS* diode, which is the trigger element, turns on first. And as soon as it injects enough current into the PNP base (N-base), the NPN turns on and then the SCR can be triggered.

3. Turn-on time definition

According to [5], the turn-on time (t_{on}) is the time required by SCR to reach full conduction after triggering. The t_{on} can be defined as the sum of: delay time, rise time and spread time. During the Delay time (t_d) the Anode current increases to 10% of its maximum value. The Rise time (t_r) is the time required for the Anode current to rise from 10% to 90% of its maximum value. During the Spread time (t_s), conduction spreads all over the area of Cathode and Anode current rises from 90% to full steady state value [6–7].

4. Investigation of existing methods to measure the turn-on time

In [2–3], two methods to measure turn-on time of SCR devices were investigated, based on TLP measurements.

The first method is based on TLP time-dependent voltage waveforms, and consists in measuring delay time from 90% to 10% of anode voltage. But in [8], this approach shows limitations related to distortions

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http://dx.doi.org/10.1016/j.microrel.2017.07.063
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Please cite this article as: M. Mahane, et al., New triggering-speed-characterization method for diode-triggered SCR using TLP, Microelectronics Reliability (2017), http://dx.doi.org/10.1016/j.microrel.2017.07.063

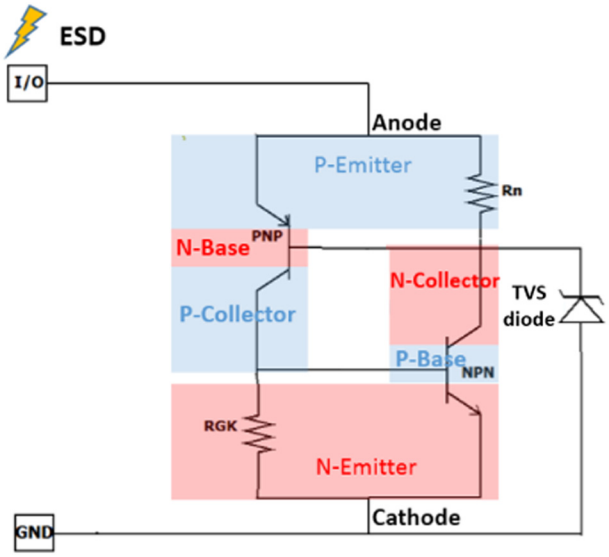


Fig. 1. DTSCR schematic representation.

of voltage waveforms due to parasitic inductance from probe needles and the clipping of the peak voltage by the TLP-tester oscilloscope. The second method is based on time-dependent current waveform to avoid parasitic inductance effects, and the turn-on time is defined from 10% to 90% of stable value of current for the holding point.

We applied this latter method to the DTSCR structure to measure the turn-on time. We used TLP system to generate 100 ns pulses, with 5 ns of rise time. The device response is recorded using a 4-GHz oscilloscope. Fig. 2 shows the resulting quasi-static I-V curve and the time-dependent voltage and current waveforms extracted from five points measurement setup: holding point (at 50 V TLP pre-charge Voltage (TLP-pchV)), two other points after turning-on (at 60 V TLP-pchV, 70 V TLP-pchV and 80 V TLP-pchV), and one point before triggering (at 20 V).

Using the current waveform at 70 V TLP-pchV, we extract the t_{on} between 10% and 90% of the on-state current value (i.e. the maximum current).

Fig. 3 shows that for the 70 V TLP pre-charge pulse, the t_{on} is sensitive to the measurement noise. Hence several t_{on} extraction windows (From 10% to 90% of on-state current value) are possible (red and green). In this particular case, t_{on} uncertainty can reach more than 200%. We also observed that t_{on} is a decreasing function of the TLP-pchV leading to a measurement dispersion higher than 15%.

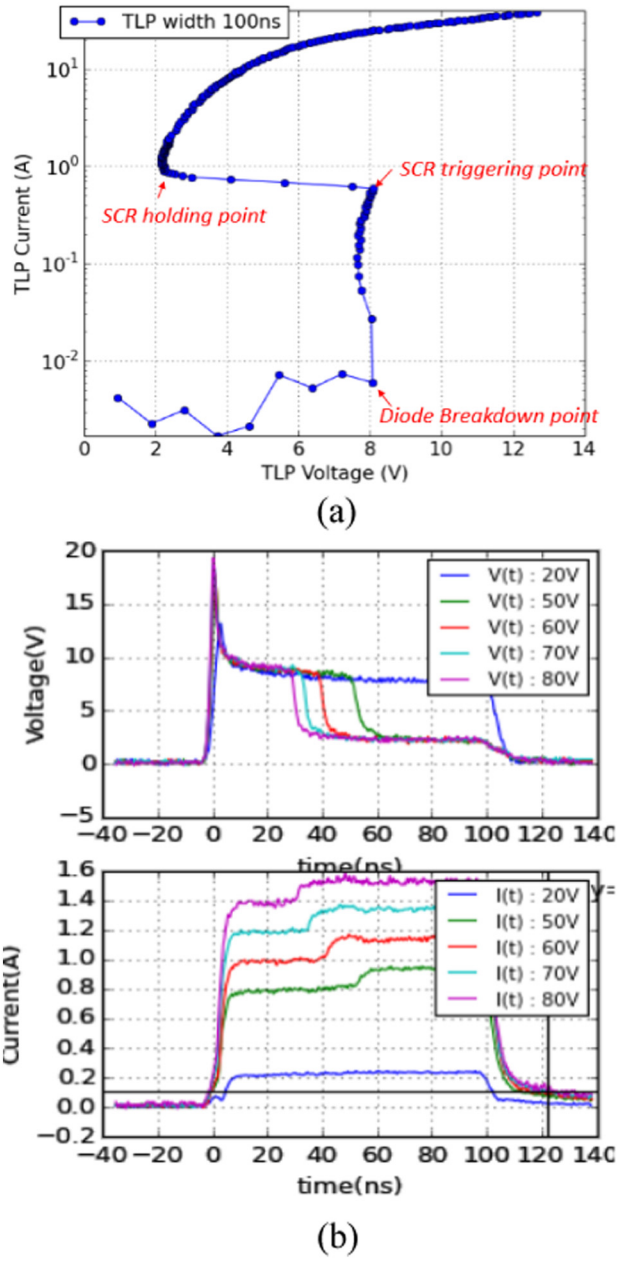


Fig. 2. (a) TLP IV characteristics of the DTSCR protection; (b) Transient voltage and current waveforms of DTSCR for different TLP-pchV (Measured by TLP with 5 ns rise time and 100 ns pulse duration).

5. Investigation of new approaches to measure turn-on time

To avoid the too large uncertainties issues on t_{on} extraction, we studied two other approaches based on the understanding of the underlying physics of SCRs triggering.

5.1. First approach: based on conductance

According to [9], during normal operation, DTSCR presents high impedance and is totally transparent for the protected circuit function. During ESD stress, once the voltage exceeds the triggering voltage, the SCR turns on and switches from high impedance (OFF-state) to low impedance (ON-state). Fig. 2 (a) shows that the DTSCR triggers on at approximately 8 V and has an on-resistance lower than 0.5 Ω. Hence, to avoid axis scaling issues due to high resistance values during OFF-state, we calculate the conductance curve of the DUT using previous voltage and current time-dependent waveforms at 70 V TLP pre-charge as shown in Fig. 4.

To filter the noise from the data, we also apply an isotonic regression (Available in Python Scikit Learn library), which smoothed data like weighted least-squares with a monotonicity constraint [10]. Fig. 4 shows the t_{on} extracted from 10% to 90% of the average conductance (red window). Hence, even if the isotonic regression minimizes the noise, and extraction uncertainty, we obtain significant differences with the t_{on} extracted from previous I (t) curve in Section 4.

5.2. Second approach: based on storage charge

The second approach of turn-on time extraction is inspired by the critical charge concept, which assumes that the thyristor is switched on when the charge of the minority carriers, stored in the bases of the thyristor, exceeds a critical charge Q_{cr} [11].

5.2.1. Turn-on time extraction from TLP results

To calculate the minimum stored charge required to turn- on the DTSCR, we apply a trapezoid integration to the previous TLP current

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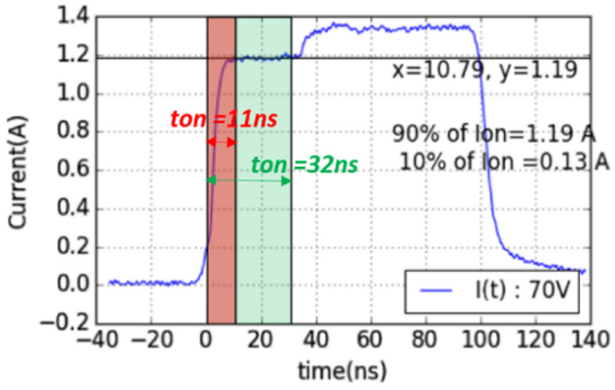


Fig. 3. Current waveforms for 70 V TLP pre-charge level and t_{on} extraction windows: For the "red" extraction window $t_{on}=11$ ns. For the "green" extraction window $t_{on}=32$ ns. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

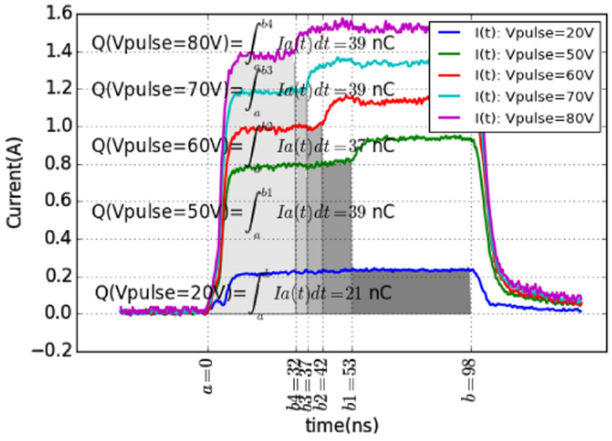


Fig. 5. The stored charge extracted from current waveforms for several TLP pulses (Measured by TLP 5 ns rise time and 100 ns pulse duration).

waveforms from the start of the pulse until the voltage drops across the device and the SCR is fully triggered on.

The resulted t_{on} versus minimum stored charge (Q) extraction is shown in Fig. 5.

It appears that even if a high current level is applied to the protection, it will not turn-on the SCR, if the generated charge in its P-base and N-base is smaller than the minimum stored charge $Q_{cr} \approx 39 \pm 2$ nC . When the stored charge is less than the critical charge, the DTSCR remains off, as we can see in the case of Vpulse = 20 V (Q = 21nC). Hence, the critical charge Q_{cr}, needed to switch-on the SCR is an intrinsic parameter describing the "sensitivity" of the thyristor [11].

5.2.2. Turn-on time extraction from IEC results

To investigate on the "universality" of the critical charge parameter, an IEC61000-4-2 characterization was performed on the previous DTSCR with minimum stored charge (Q) extraction (Fig. 6).

The results show that the device turned on once the same stored charge (previously extracted from TLP) is reached, resulting in a decreasing of voltage drop. Hence, the Q_{cr} critical charge parameter is a DUT specific parameter, which is independent of the stress source impedance (IEC, TLP…).

6. TCAD simulation: turn-on time extraction from TLP results

To assess the stored charge approach for evaluating the turn-on time, we investigate the turn-on mechanism of the DTSCR during a TLP stress by implementing a 2D simulation using TCAD tool. The model was first calibrated using a standard procedure. The physical models used for DTSCR simulation are Phumob model for generation, Auger recombination for highly doped regions and SRH recombination, with Doping, Temperature and Electric field dependence. The Carriers mobility depends on the doping profile and the electric field.

The resulted t_{on} versus minimum stored charge (Q) extraction is shown in Fig. 7.

It appears that transient simulation current waveforms closely match the TLP measurements, despite a faster turn-on time and critical stored charge ($Q_{cr} \approx 20 \pm 2$ nC) compared with the experimental results. We are currently investigating whether this type of measurement could be useful to better calibrate the simulator.

Fig. 8 shows schematically, the excess charge distribution in all four regions of the DTSCR structure at 30 V TLP pre-charge during seven phases of the triggering process.

When the SCR is forward biased, the P+ Emitter/N-Base junction (J1) and the N+ Emitter/P-base junction (J3) become forward biased whereas the central junction between the P-base and the N-base regions (J2) becomes reverse biased [12].

At t0, a TLP pre-charge is applied to the DTSCR.

During the interval from t0 to t4 of Fig. 8(a), diode breakdown occurs, and a gate current is injected into the N-base of the PNP transistor, promoting hole diffusion from the junction J1 into the N-base. This current is partially used for storing a charge called the "Normal Forward" charge $q_{N,pnp}$. Thus, the width of the un-depleted portion of the N-Base region becomes smaller. Once the injected holes enter the P-

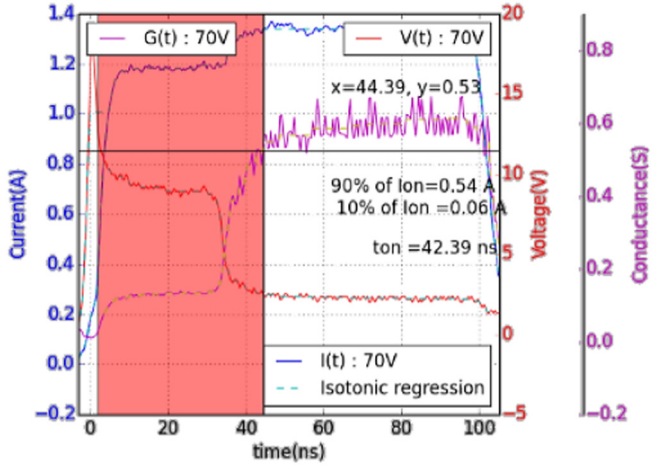


Fig. 4. Isotonic regression [10] performed on current, voltage, and calculated conductance waveforms (At 70 V TLP pulse).

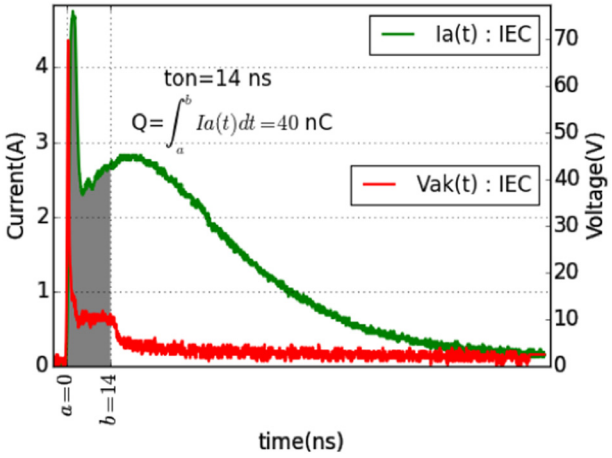


Fig. 6. The turn-on time of DTSCR protection, extracted from IEC current waveform at 1.5 kV level, using the stored charge method.

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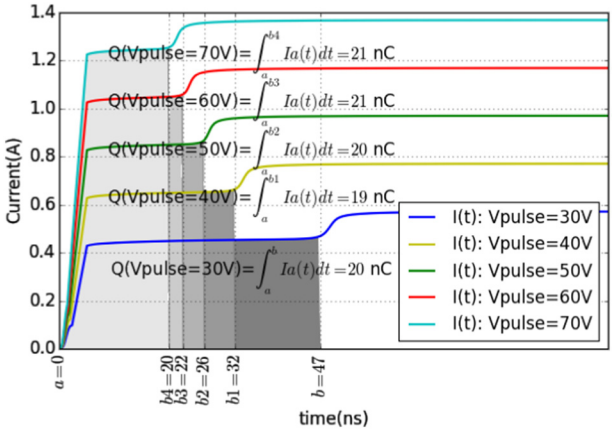


Fig. 7. The stored charge extracted from current waveforms simulation of DTSCR structure for several TLP pulses (TLP 5 ns rise time and 100 ns pulse duration).

Base, they promote electrons injection from the junction J3 into the P-Base, leading to electrons minority carriers stored charge in the P-Base called the "Normal Forward" charge $q_{N,npn}$.

At time t4, a small area of the blocking junction J2 is saturated with injected minority carriers. Hence the diffused electrons from N+ emitter enter the N-Base region, creating a base drive current for the PNP transistor, which promotes more hole injection from the P+ emitter into the N-Base [12]. Thus, an additional charge into N-Base and P-Base regions is injected due to the collector currents of the two bipolar transistors. This charge is called the "Saturation" charge $q_{S,pnp}$ and $q_{S,npn}$ in N-Base and P-Base respectively.

Therefore, as shown in Figs. 8(a) and 9, the total stored charge in both bases can be expressed by [13]:

$$q_T = q_{B,pnp} + q_{B,npn} \tag{1}$$

with

$$q_{B,npn} = q_{N,npn} + q_{S,npn} \tag{2}$$

$$q_{B,pnp} = q_{N,pnp} + q_{S,pnp} \tag{3}$$

At t4, the total stored charge reaches the minimum critical charge required to turn on the thyristor. In fact, a much larger concentration of electrons is supplied to the N-Base of the PNP transistor than required to operate in the active mode, forcing the PNP transistor into its saturation region [12]. This increases the growth of the stored charge within the bases, promoting the internal feedback mechanism between the NPN and PNP transistors. Hence, the switching, which primarily initiates as a current filament in the junction J2, spreads across the whole area of the junction during interval t4 to t5. Consequently, all three junctions of the DTSCR operate in forward bias, hence the current flowing through the thyristor increases to a steady level (limited by the external circuit) and a small forward voltage drop across the device remains as shown in Fig. 8(b).

Based on the charge control model [9], the increase of the anode current during the turn-on process is given by:

$$J_A(t) \propto J_G \left(e^{\frac{t}{\sqrt{t_{B,npn} \cdot t_{B,pnp}}}} - 1 \right) \tag{4}$$

where J_A is the anode current density and $J_G$the gate current density. The rise time from 0 to 90% is proportional to the time constant [9]:

$$t_{on} \propto \sqrt{t_{B,pnp} t_{B,npn}} \tag{5}$$

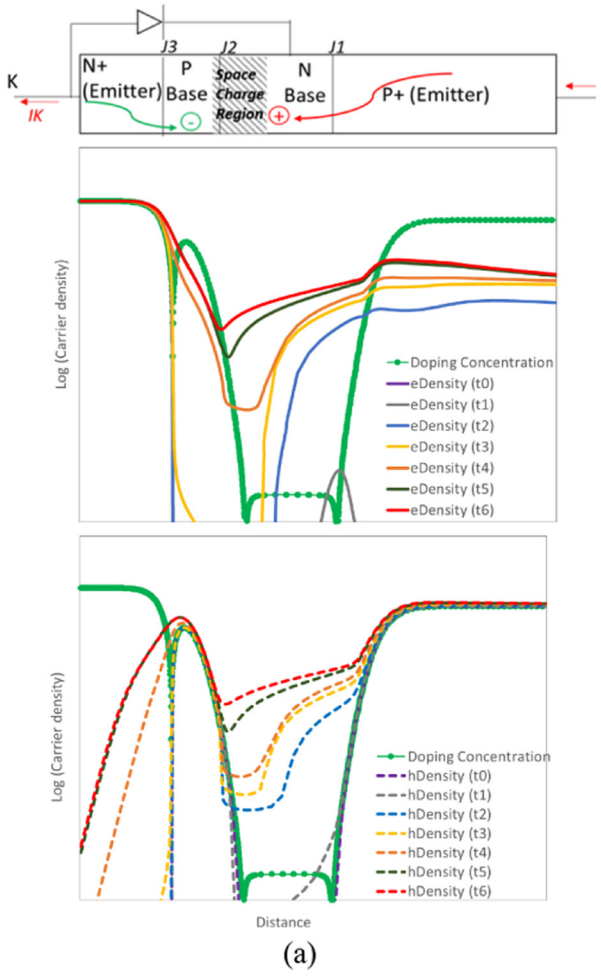


Fig. 8. (a) Growth of the concentration of minority carriers in DTSCR during the triggering process under TLP pre-charge = 30 V, (b) Growth of the stored charge extracted from current waveform simulation of DTSCR structure at 30 V TLP pre-charge.

Fig. 7 shows that the turn-on time of the DTSCR is a function of the anode bias, while the critical charge stays constant. In fact, a higher anode bias induces a thinner un-depleted region of N-Base [14], which decreases the minority carrier transit time in the structure and increases the emitter PN junction current density. This implies that a much larger charge of minority carriers is injected in the bases of the thyristor reducing the time over which critical charge Q_{cr} is established. The DTSCR is therefore, forced into the on-state at lower turn-on time.

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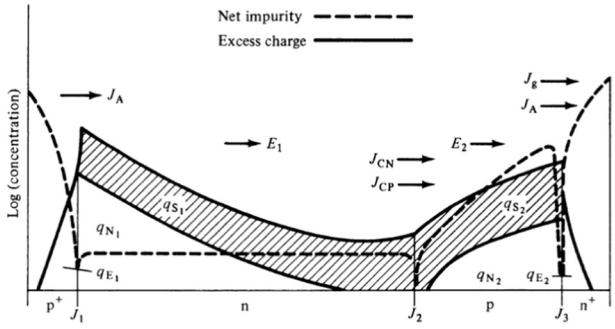


Fig. 9. Forward-conduction charge model of a P-N-P-N device [9].

7. Comparing devices turn-on time performance using stored charge extraction method

Based on [11], if the gate current slowly grows, the SCR is turned on at the point where the minority carrier charge density has a maximum and it is equal to the critical charge Q_{cr} represented by:

$$Q_{cr} = j_R \times t_r \tag{6}$$

where j_R is the leakage current density of the emitter PN junction (J1), which depends on gate current pulse duration and density that can switch-on the thyristor. The t_r is the switch-on current rise time.

Based on [9–15], for a very crude estimation, the rise time taken by the anode current density to increase from the 0 to 90% level is proportional to the time constant:

$$t_{on} = t_d + t_r \propto \sqrt{t_{B,pnp} t_{B,npn}} \tag{7}$$

where $t_{B,pnp}$ and $t_{B,npn}$ are the P-base and N-base transit times, and can be approximated as follows [15]:

$$t_{B,pnp} = \frac{W_P^2}{2D_N} \text{ and } t_{B,npn} = \frac{W_N^2}{2D_P} \tag{8}$$

where D_N and D_P are the diffusion coefficients of electrons in P-base and holes in N-base, respectively. W_P and W_N denote the base region widths of the P-base and N-base, respectively.

Based on this approach, the t_{on} of the DTSCR protection is design and process dependent. So t_{on} can be reduced by making faster PNP and NPN transistors through narrower or more highly doped N-Base and P-Base regions.

In Fig. 10, the turn-on speed of two DTSCR structures with two different N-base spacing are investigated. We measured DTSCR t_{on} using TLP current waveforms, in the case of fast and slow PNP transistor (thinner and wider N-Base, respectively). We observed that a minimum stored charge Q_{cr} is required to turn-on the SCR ($Q_{cr} \approx 4$ nC for thin N-Base and $Q_{cr} \approx 12$ nC for the wide N-Base). Hence the narrower is the N-base, the shorter is the time required to diffuse the carriers through the base, and the lower is the critical charge required. At 19 V pre-charge TLP pulse, the turn-on time t_{on} of the SCR decreases from 87 ns to 27 ns for wider and thinner N-Base, respectively.

8. Conclusion

According to measurement results, the stored charge is a specific parameter of each thyristor structure, which depends on design and process parameters whereas the turn-on time is dependent on the way the device is biased. The critical charge allows to measure the turn-on time for low currents and extrapolate it to high currents levels, which are more sensitive to the parasitic effects of the TLP equipment. Considering the critical charge as an intrinsic parameter of the thyristor, the triggering-speed performance of different structures could be compared by extracting their specific minimum stored charge, once the structure is fully triggered, using time-dependent current TLP waveforms as proposed in this work: the lowest is the minimum stored charge, the faster is the triggering.

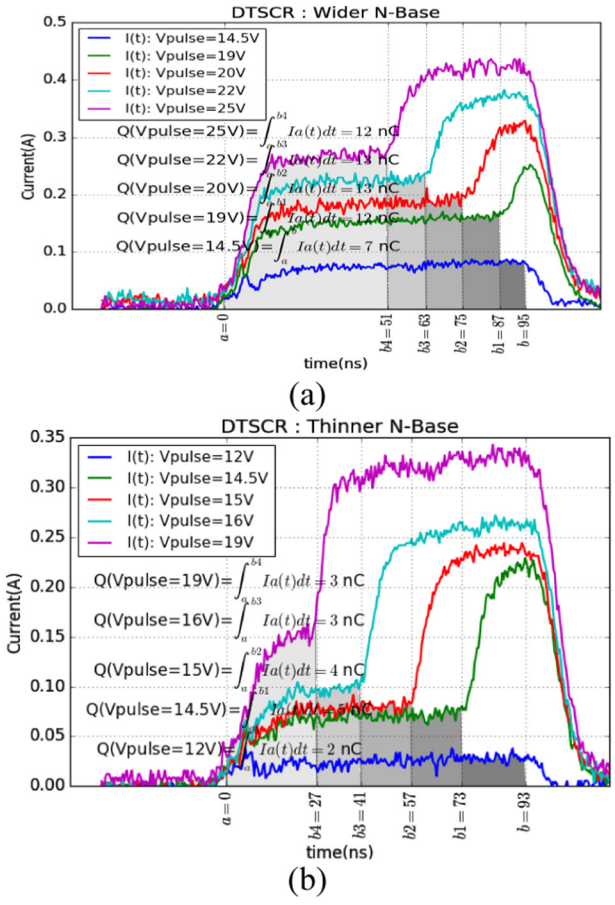


Fig. 10. Compared t_{on} extracted from TLP-measurements ($t_{rise}=5ns$, $t_{width}=100ns$) transient current waveforms of high sensitivity and low sensitivity DTSCR for two TLP levels. Plot (a): High sensitivity DTSCR turned on in 73 ns at 14.5 V TLP pre-charge while low sensitive DTSCR is still OFF. Plot (b) Low sensitive DTSCR turned on in 87 ns at 19 V TLP pre-charge for higher critical charge.

Acknowledgment

The authors would like to thank E. Bouyssou for reviewing and monitoring the paper. And Y. Buvat for characterization support. Special thanks to the French National Association for Research and Technology for continuing to provide support for researchers through scholarship programs.

References

[1] R. Gauthier, M. Abou-Khalil, K. Chatty, S. Mitra, J. Li, Investigation of voltage overshoots in diode triggered silicon controlled rectifiers (DTSCRs) under very fast transmission line pulsing (VFTLP), 2009 31st EOS/ESD Symposium, Anaheim, CA 2009, pp. 1–10.
[2] M.X. Huo, et al., Investigation of turn-on speeds of electrostatic discharge protection devices using transmission-line pulsing technique, 2008 2nd IEEE International Nanoelectronics Conference, Shanghai 2008, pp. 601–606.
[3] M. Mergens, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, R. Mohn, B. Keppens, C. Trinh, Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides, IEDM. Proc. 2003, p. 515.
[4] B. Wong, A. Mittal, Y. Cao, G.W. Starr, Nano-CMOS Circuit and Physical Design, John Wiley & Sons, 2005 200.
[5] U.A. Bakshi, A.P. Godse, Electronic Devices and Circuits, Technical Publications, 2009 85.
[6] B.M. Reddy, M.A. Prasad, S. Sivanagaraju, Power Electronics, Prentice-Hall of India Pvt. Ltd., 2010 16–17.

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[7] J. Arnould, P. Merle, Dispositifs de l'Electronique de Puissance, HERMES edition2, 1992 237–239.
[8] M.x. Huo, et al., Study of turn-on characteristics of SCRs for ESD protection with TDR-O and TDR-S TLPs, 2010 17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, Singapore 2010, pp. 1–8.
[9] A. Blicher, Thyristor Physics, Springer Verlag, New York, 1976 46–280.
[10] M. Bommarito, http://bommaritollc.com/2014/06/08/isotonic-regressions-scikit-learn/ June, 2014 [August 14, 2016].
[11] M. Shur, S. Rumyanstev, M. Levinshtein, SiC Materials and Devices, 1, World Scientific, Singapore, 2006 931–981.
[12] B.J. Baliga, Fundamentals of Power Semiconductor Devices, Springer-Science, New York, 2008 651–653.
[13] R.L. Davies, J. Petruzella, p-n-p-n charge dynamics, Proc. IEEE 55 (8) (Aug. 1967) 1318–1330.
[14] B.J. Baliga, Advanced High Voltage Power Device Concepts, Springer-Science, New York, 2011 27.
[15] S.M. Sze, Physics of Semiconductor Devices, 2nd ed. John Wiley & Sons, New York, 1981 214.

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