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# LIN communication behaviours against ESD events

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**Abstract**— An automotive application can see several perturbations during his life. In this paper we study how the LIN communication under ESD stress behaves and what sort of failures could be observed. We proposed a characterisation method in order to quantify soft failures. These different failures are classified following a criteria defined in the document. A susceptibility level for the LIN communication depending on the ESD stress level and duration are extracted and implemented in simulation as a failure block.

**Keywords**— Automotive communication; LIN (Local Interconnect Network); ESD (Electro-Static Discharge)

## I. INTRODUCTION

The automotive industry includes more and more electronic systems that give better functionalities and security. For safety reasons, the electronic implementation and the embedded ICs (integrated circuit) are more concerned by the robustness and reliability. In operating conditions, cars are exposed to external perturbations, such as vibrations, high thermal variations and also ElectroMagnetic Interferences (EMI). As the systems are not directly connected to ground, fast discharge events due to electrostatic accumulation or disconnection of cables can induce Electrical Fast Transient (EFT) perturbations. These perturbations can induce critical fault in the automotive application and impact on the safety of the passengers.

In an automotive system, up to 50 to 100 Electronic Control Units (ECU) can be implemented each one referred to computers or the assembly of several of individual control modules. All these ECU are connected together in a complex multiplexed network using different protocols such as Local Interconnect Network (LIN) or Control Area Network (CAN). These protocols are self-protected and enable reliability into the communications.

In this paper, we study the impact of the EFT on the LIN component. This component is a reference in automotive communication applications. There are several LIN component manufacturers, we choose three of them named A, B and C. We know that each manufacturer has its own IC's protection strategy that is studied in the first part using the SEED methodology [1]. Based on [2], two kinds of failure can be studied, the first one called "hard failure", is the destruction of the IC, already mentioned in [3] [4]. We are now focusing on the "Soft Failure" [5] [6] [7] [8] which relates to functional problems such as the lost of clock, RESET, etc... In our study, we focus on communication problem that induced the loose of information on the LIN, due to an EFT event. EFT events are really different than EMC stresses. The high level of injections (some KVs, some 5A to 30A), on short times (hundreds ns), triggers the on-chip ESD protections, connecting the output to ground or to VDD depending on the ESD strategy used by the

manufacturer. Regarding EMC DPI or field susceptibility methods, it never happens on such automobile components.

A board has been developed to characterize each LIN in "normal mode" with the maximum data rate, 20Kb/s. We used a TLP (Transmission Line Pulse) generator, to reproduce an EFT event on the LIN Bus. This study determines the level of susceptibility for one LIN without external component. In the next step, we connect two LINs, one as a Master and the other one as a Slave, and we extract the new susceptibility level for each combination Master/Slave, with these three LIN manufacturers. Thanks to this study, we would like to report the mistakes that a very short EFT stress can introduce into a communication link. One of the main objectives is to classify the failures, related to the on-chip ESD protection strategy, and to define some criteria for computing prediction. These criteria will feed the standards under development on the WG26 ESDA (ElectroStatic Discharge Association – WG system level models) and of the IEC 62433-6 standard under development.

## II. SYSTEM UNDER TEST

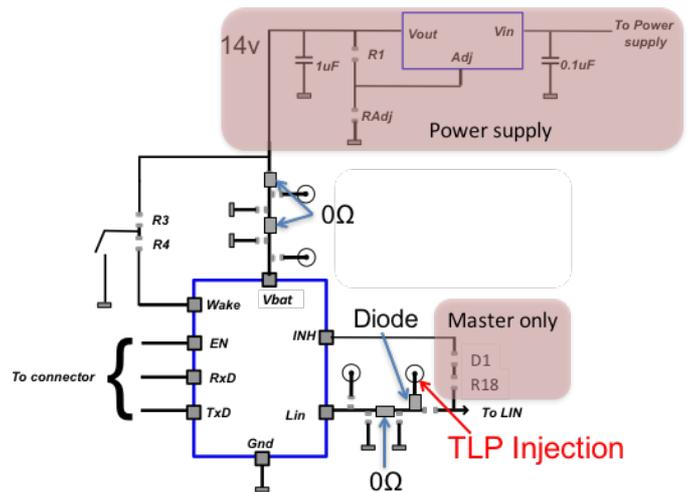


Fig. 1. Schematic of LIN board

Following the schematic Fig.1, the board includes a power supply part. The LIN can work with power supply, Vbat, from 7V to 27V. For this study, we fixed it to 14V, closed to the batteries voltage under normal operating condition in vehicles. The same pattern to inject a stress and to measure is placed both on the LIN input and the Vbat pin. This pattern allows us to have a local monitoring, but also to add some external components as described in [2]. To inject the stress a diode is used on this injection pattern (between the TLP injection and LIN pin on Fig.1)

To reproduced EFT, we used a TLP generator made of a 50Ω transmission line. The length of line determines the pulse width. Four different pulse widths were used (50ns, 100ns, 200ns and 300ns). A high-voltage alimention charges the line. The TLP generator can reach 2000V on 50Ω that means 40A during the pulse.

Using TLP generator we extracted the behaviour of the LIN-GND ESD protections of the three LIN samples when the LIN output is in High level and Low level. Results of the 3 devices are reported in Fig.2. As shown, whatever the output level (high or low), the I(V) quasi-static curves follow the same shape.

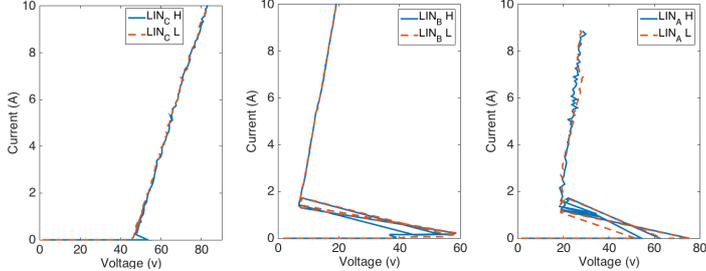


Fig. 2. IV quasi-static LIN-GND curves for each manufacturer tested in both state of LIN pin

To investigate soft failure of each component, the component is in “slave” mode (without R18 and D1 - Fig.1), and we configure it into “Normal” mode. The setup is reported in Fig.3. Through a regulator, 14V DC is applied to the power supply pin (*Vbat*) and 5V to *En* pin (that enable the LIN driver and configure the “normal” mode). The *Tx* pin is connected to the TTL output from the 8110A pulse generator. This output represents the 0-5v information from the microcontroller, sent to the *LIN* pin, at 10Khz with 50% duty cycle (max rate data 20Kb/s). The driver, write on the *LIN* bus, all information from *Tx* a few microseconds later (levels: 0-14V). *Rx* pin is the image of the information transmitted on the bus read by the driver and returned to the microcontroller for verification. Three voltage probes allow us to control *Tx*, *Rx* and *LIN* on the oscilloscope. The TLP injection is performed to the *LIN* pin trough a diode.

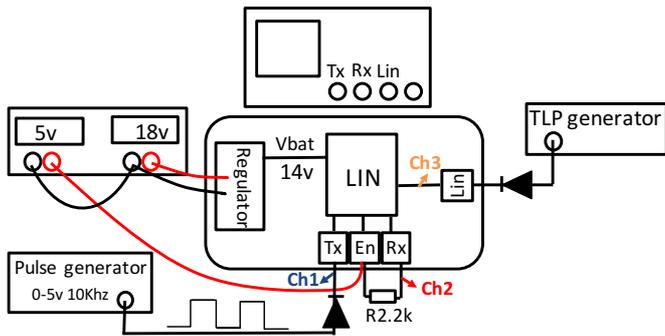


Fig. 3. Schematic of the test bench to charaterize one LIN

### III. LIN SOFT FAILURE MEASUREMENTS

Among the numerous results, the highlighted measurements results are reported bellow. In Fig.4, the TLP (8A-300ns) activates the EFT protection that drives the LIN down to zero during a short time. It doesn't impact the Rx signal and no failure is noticed on this case. In Fig.5, the TLP (16A-200ns

duration) appears during high level and activates the LIN-GND protection that drives *LIN* to a low state during around 5μs. The *Rx* pin follows and reports a failure to the microcontroller.

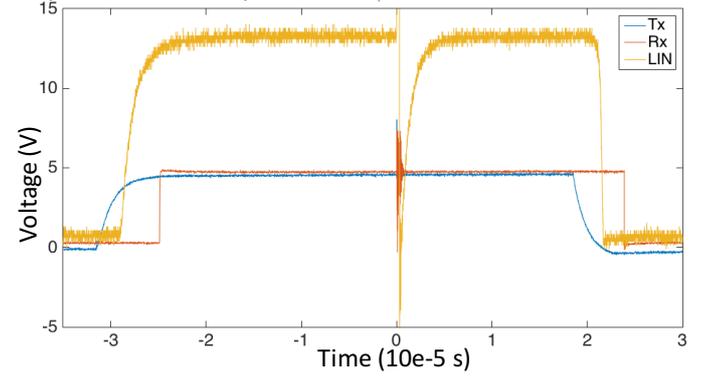


Fig. 4. LIN C with a perturbation at times 0, the TLP generator is set with 8A for 300ns pulse wide

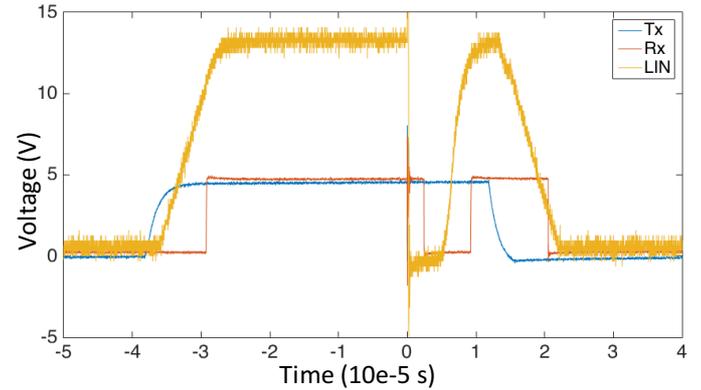


Fig. 5. LIN A with a perturbation at times 0, the TLP generator is set with 16A for 200ns pulse wide

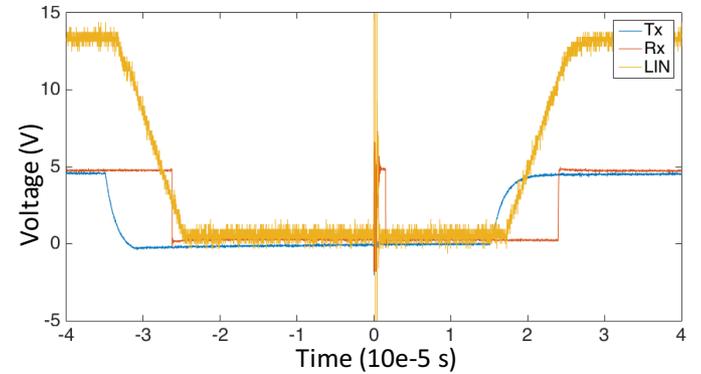
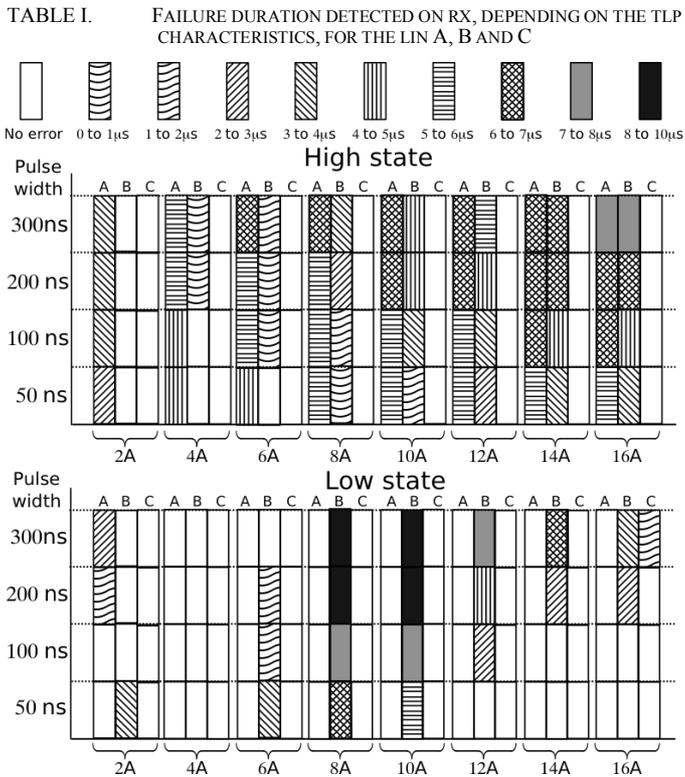


Fig. 6. LIN A with a perturbation at times 0, the TLP generator is set with 2A for 200ns pulse wide

When the TLP (100V-200ns) stress arrives during low state Fig.6, no change is observed on *LIN* pin, but Rx reports a failure for few μs. All perturbations ( amplitude and duration) that create a *Rx* state change are summarized in table.I. The failure duration are reported (depending on their severity), regarding the TLP amplitude (A) and TLP duration (50ns, 100ns, 200ns and 300ns) for both high and low level. One colon represents the observable fault for one component (A, B or C) depending on the pulse width for a give current injection level.

Ten severity levels of failures are reported from “No error” (white), to more than 8 $\mu$ s data error on the RX pin of the LIN device (Black) on the top of the figure. First graph gives the errors while the output state of the LIN bus is at High level, the second one for Low level.



Different observations can be done on these results.

When the LIN is in high state:

- For 2A injection, only the component A failed with an error duration between 2 and 3 $\mu$ s for a 50ns pulse width, and with an error duration between 3 to 4 $\mu$ s duration for an injection pulse duration of 100ns, 200ns and 300ns. No error is observed on component B & C.
- When the level of injection increases, the severity of the failure increases on component A & B. Such results is a behavior that would have been expected: when the energy of the stress increase, the failure level increases.
- Concerning component C whatever the level of injection, no error is observed.

When the LIN is in low state :

- If a stress occurs at low state, we can notice fewer errors than in high state. Focussing on the low level of TLP injection, errors are seen for 2A on component A & B: For 200ns and 300ns pulse width with component A and only for 50ns duration with component B.
- Surprisingly, component A doesn't have any error for higher injections.
- The higher failure level is observed on component B with injections around 8-10A, and then it decreases for more power full injections. Such results are not what we was

supposed to see and it does not follow the behaviour of the High level state.

- The only failure on component C is observed for the most critical injection done: 16A, 300ns. We can wonder why this component is even more robust than the two other ones. Looking at the signals into detail, even on component C, errors can be observed on the LIN bus. But it seems that the architecture of component C have an on-chip data correction system, because all these errors are not reproduced on the RX pin, while components A & B reproduce what is observed on the LIN bus.

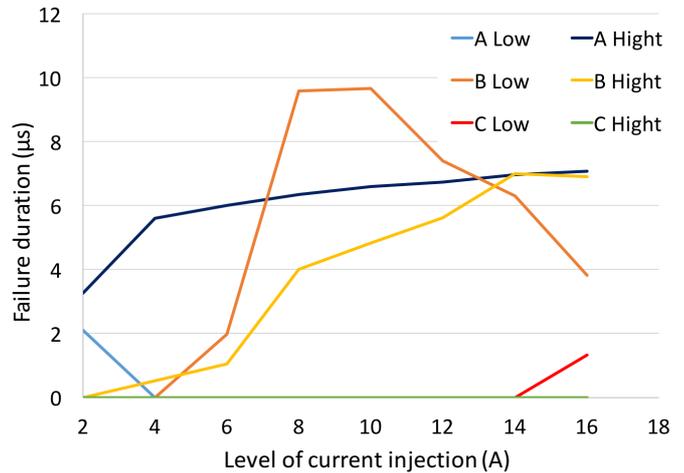


Fig. 7. Failure duration depending on current injection for a pulse wide of 300ns.

Each component A, B and C are tested following the same configuration. Depending on the manufacturer, the failure types are not the same, example *Fig.7* we compare the susceptibility level for each component at both state for a 300ns TLP. It seems that the response of the component to the same stresses depends on the on-chip ESD strategies used and on the LIN state.

#### IV. CHARACTERISATION LIN NETWORK

In automotive application, the LIN bus is composed of one master LIN and several slaves. On different configurations, mixing LIN A, B and C, we monitor the Rx1 from the master the Rx2 from the slave and the LIN bus. The whole setup is reported in *Fig.8*. A twisted cable link the LIN bus of two boards and the TLP injection is done on the LIN bus, closed to the master while a message is sent.

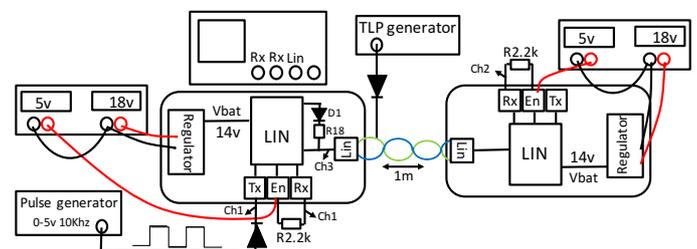


Fig. 8. Schematic of the test bench for LIN network characterization

Some interesting malfunction during the communication, between the LIN C master and the LIN A slave, are reported bellow *Fig.9*. The EFT arrives at times 0, when the LIN is in low state. After this perturbation, the LIN is stuck in high state instead of low and the message is delayed. *Table.II*, reports the severity of failure when the stress occurs while the output is at low level. We report the failure duration seen on both sides, master (M) and slave (S). For pulse duration of 300ns, hard failure is observed. It has to be noticed that both the device are able to resist to much more higher stresses (20A instead of 16A). The operating conditions influence the severity of failures. This is the only combination that drives to hard failure.

TABLE II. SUSCEPTIBILITY LEVEL FOR THE LIN COMMUNICATION BETWEEN THE MASTER (LIN C) AND THE SLAVE (LIN A)

					HF
No error	0 to 1μs	some μs	more than 8μs	some ms	Hard Failure

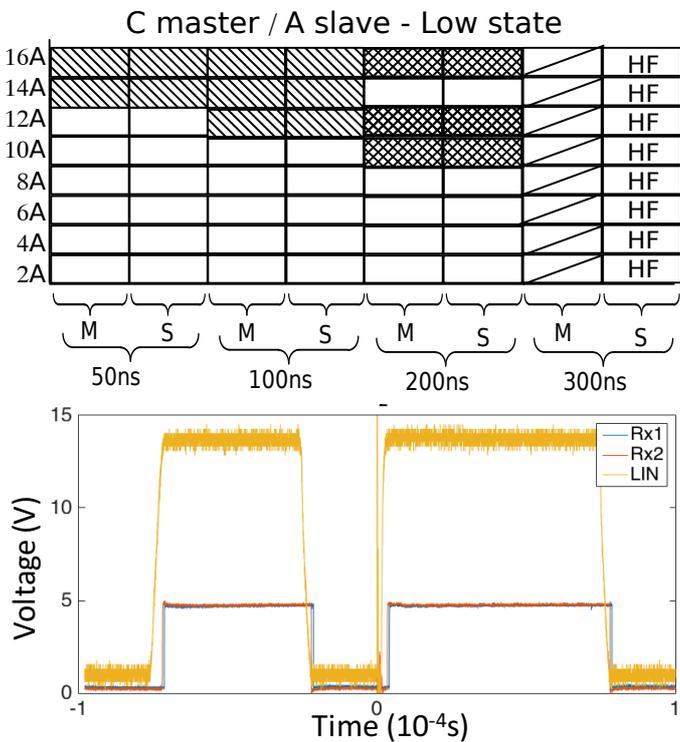
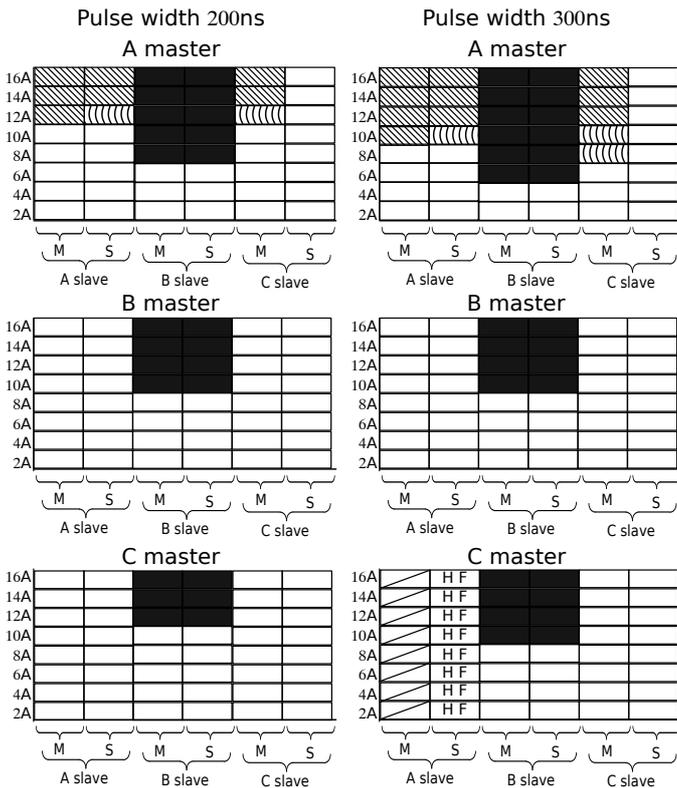


TABLE III. SUSCEPTIBILITY LEVEL OF THE HIGH LIN STATE BETWEEN THE MASTER AND SLAVE FOR ALL COMBINATION



How to read these tables: Each colon represents the failure observed following the severity reported in table II. As an example, graph on left top reports the failures while component A is in master mode. The pair of colons (M & S) reports the configuration where A, B, and C are in slave mode respectively from left to right. Colon on reports the failure on master and colon two on the slave.

In table III (High state) it appears that whatever the component set in master mode, when the component B is set in slave mode the robustness of the LIN communication is decreased. Both master and slave exhibit a strong error. When B is in master mode (Bm) link to component A or C (As or Cs), no error is observed.

The most robustness cases are when we used two C components (Cm-Cs), Bm-As or Bm-Cs, no error are observed for both pulse width. We can't observe what happens on the master because the LIN communication shut down due to the short-circuit created by the slave.

Component C in master mode combined with A in slave mode (Cm-As) conducts to hard failure for 300ns pulse width but no error for 200ns duration.

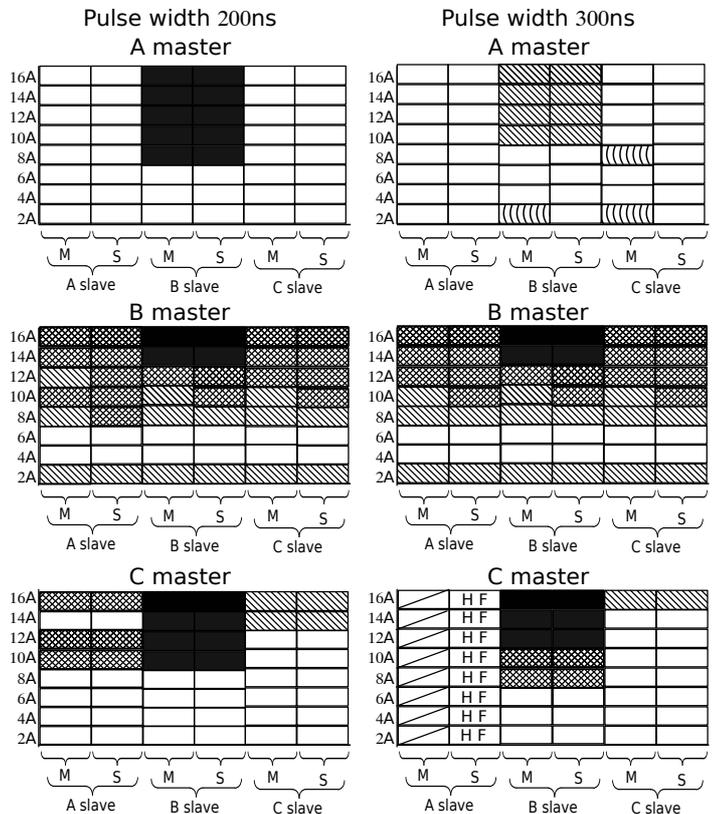
The worst case is the Am-Bs, the communication is lost during "some ms" for 8A injection and more.

The combination Am-As or Am-Cs have a susceptibility level which decreases when the pulse duration increase from 200ns to 300ns.

- From 12A to 10A for Am-As, the As loses the communication during "less than 1 $\mu$ s" to "some  $\mu$ s" for the higher injection. The Am loses the communication during "some  $\mu$ s" above this susceptibility level.

- From 12A to 16A for Am-Cs, no error is detected on the slave (Cs) for both pulses duration. The A master component had an error duration "less than 1 $\mu$ s" to "some  $\mu$ s".

TABLE IV. SUSCEPTIBILITY LEVEL OF THE LOW LIN STATE BETWEEN THE MASTER AND SLAVE FOR ALL COMBINATION



When the LIN is in low state, things look different...

When component B is set in master mode (Bm), all injections except for 2A and 4A, report an error.

Refer to *table.I* for the component B alone under 12A injection with 300ns of pulse width, we get an error duration between "7 $\mu$ s to 8 $\mu$ s". Using the combination Bm-Bs, we have placed exactly the same protections in parallel (on both side of the cable). we get for the same injection an error duration "more than 8 $\mu$ s". This error is not divided by twice due to the propagation on the twisted cable. The phenomenon is much more complex then expected and is difficult to conclude without taking into account the transient waveforms on both sides of the cable.

Regarding these tables, it can be noticed that the failures level is very different depending on the combinations found on the LIN: manufacturers, master of slave mode). The most surprising thing is that no link appears between a characterization of the stand-alone components and in system configuration.

It is not clear that is only due to the ESD protection strategy used by each manufacturer. At this moment it seems difficult to simulate such malfunction using the SEED methodology or to create models that can predict systems. In system configuration hard failure can appear even if it does not exist when the component is tested alone.

We need more investigation to develop a model which can take into account both “hard” and “soft” failure. This work is in process in the ESDA working group 26.

## V. CONCLUSION AND PROSPECT

A study of different LIN manufacturer components stressed by a TLP during a basic communication, allows showing the different communication malfunctions. We proposed in this paper a characterized method to define the susceptibility level of the different LIN, to establish a failure criteria on stand-alone components, even if the failures can be very different depending on the ESD chip’s strategy. This work also demonstrates that two different LINs communicating together decrease the threshold of susceptibility. It is difficult to see a direct link between stand-alone failures and system failures

The main objective of this work is to create a model which take into account all parameters measured. This full behavioral model will be based on the ESD protection strategy and on failure blocks (FB) that include probability levels of failures as previously studied in [8].

## **Acknowledgment**

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