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Low stress polyimide multilayers integration for flexible substrate

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Abstract

Materials integration in flexible substrate to do foldable and bending MEMS or electronics devices seems to be required for a lot of applications. That's why; we present here a simple fabrication process flow to make polyimide (PI) devices easily peelable from a rigid support host. Besides the PI flexible device keeps its original aspect thanks to the hygroscopic character of the carrier [1]. The advantage of this process is its simplicity of implementation on a support host without sacrificial layer. It makes it possible to control roughness, deposited thickness, and also to limit the constraints between various materials.

1 Introduction

In many cases, structures realized on flexible polymer, like Polyimide or Polyethylene terephthalate (PET), can be obtained by lamination of a commercial polymer film like Kapton® (usually sold in rolls) on a host support covered with a double-sided adhesive or a thin sacrificial layer. In this way we can produce monolayer devices, using unitary procedures of metallization and passivation with a low resolution of alignment.

Since it's not possible to control the mechanical keeping of the support during the various chemical and physical steps of the process the handling become very tricky.
Moreover the modification of the mechanical properties induced by the technological steps leads to a loss of resolution and precision during the photolithographic alignment phase. For all these reasons it's practically impossible to achieve multilayers devices with high resolution using this materials.

To attain new technologies in this field, it's first of all necessary to get rid of the commercial film and realize deposit of polymer starting from a commercial resin for spin coating purposes. There are in fact many drawbacks linked to the use of commercial Kapton® like inhomogeneity of the film thickness, scratches on the surface, or even the use of an adhesive layer like Polydimethylsiloxane (PDMS) layer needing special equipment for chemical handling and annealing temperatures of the PDMS. This last parameter is a very limiting factor for structures production that

implying alignment of several photolithographic levels and achievement of few micrometers of resolution.
In this work we have realized a simple protocol for the development of multilayer structures in polyimide with high resolution and very low roughness (similar to that of silicon), easily detachable from the rigid support host for achieving of highly flexible and biocompatible structures suitable for body implant applications.

2 Realization

2.1 Polymers Materials

PI used are PI2611 (thermally curable) and HD4110 (photo definable) from HD Microsystems. They are known for their excellent mechanical and chemical resistances, high glass transition temperature, biocompatibilities [2], dielectric properties, and so on. Moreover, they have thermal dilation coefficients (3ppm/°C) close to the silicon which make it possible to reduce the stress throughout the process fabrication and to built or integrate MEMS or electronics devices.

2.2 Process Flow

A process fabrication procedure (Fig. 3) to realize a 25µm double face patterned structure in polyimide is done on a standard silicon substrate hydrated beforehand with a 200nm thick of silicon oxide (a). There are different procedures following the PI used. For the PI2611 (b'), the first layer deposited by ring must be lower than 4 µm to guarantee the mechanical resistance of this one on the substrate. An annealing of the PI at 350°C during 30 minutes on an oven is recommended in order to obtain all the physical and chemical optimum characteristics of the material. Then the opening vias are done by PI etching with O2 (80%) and CF4 (20%) plasma through a patterned positive resin. For the HD4110 (b), we use an adhesion promoter (VM651 from HDmicrosystems) before its spin coat. Then we do the openings vias on it by photolithography using a MA150 aligner. An annealing of the PI at 350°C on an oven during 30 minutes is done like PI2611. Then, the procedure is the same for both PI. We do a metal deposition ((c) Ti 50nm/Au 400nm) by evaporation on the entire surface. A positive resin ((d) AZ40XT 13µm) was patterned on the top for the vias filling (e) by electrodeposition. The bumps are made in gold with a thickness of 4µm to 9µm corresponding to the thickness of the vias. The resin is then dissolve and another one (ECI 1.2µm) is patterned to define the current lines by gold and titanium chemical etching (f). Then, we do the same steps as previous in order to build a complete structure with opening contacts on both sides (g,h,i). Small oxygen plasma is needed (2min@100W) to ensure the PI layers between each others.

The peeling of the flexible substrate of PI (Fig.4) is done by separation out of ring on the entire periphery of the silicon wafer for PI2611. To separate the HD4110 structure

from is support we need to deep it in HF solution to remove the silicon oxide. A cutting of the wafer unit/polyimide can also be done with a diamonds saw or by laser.

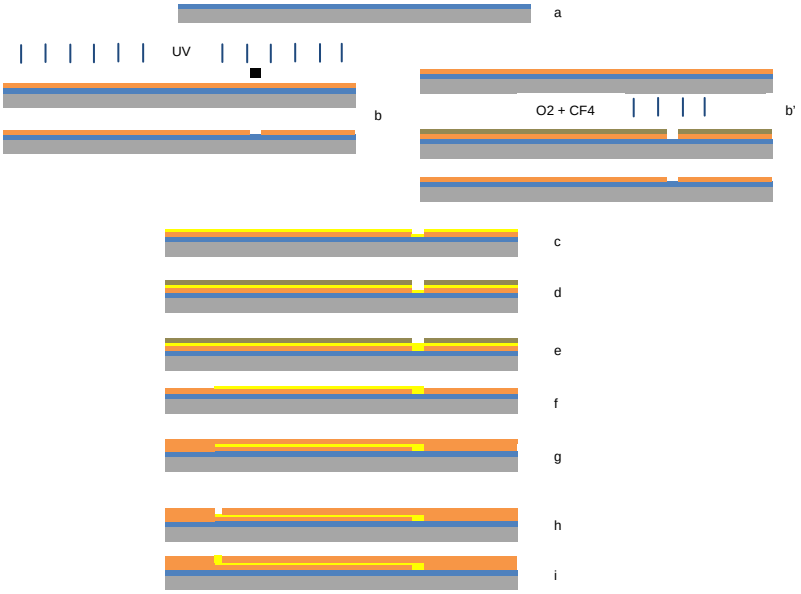


Fig.3: Overview of the process flow integration



Fig.4: PI final structure (25µm)

A minimum adhesion of the polyimide on silicon allows the stacking of several layers of those while keeping the flatness and the initial silicon stress. Thin or large PI deposit layers can be stacked by spin coating or by screen printing (to avoid plasma etching) depends of the relief and the area to be treated. Flatness and low stress allows integration of conducting, resistive or passive material in or on this flexible substrate to define sensor, actuator or sensitive area. Different deposit technique can be used following the resolution and desired thickness.

3 Results

We have done the fabrication of 25µm thickness double face patterned flexible structure. We used for that two different polyimide with two different techniques. Both of them are similar and the results are the same. We obtain flexible structure with electrical contacts on both sides. The difference is essentially on the drilling for the vias. For the PI2611, we improved its etching with RIE equipment. We used a 5µm positive resin as masking to etch 4µm PI2611. For the HD4110, we optimized the lithography process (multi soft bake, isolation time, N2 purging after UV, PEB, latent time before developing) to have straight flank, good adhesion on the substrate and to increase the resolution.
Then the others steps are the same for the two polyimide. We improved the adherence between each PI layer by using small plasma O2 to increase the roughness of them. We optimized the thickness PI deposition to ensure the good

filling of the vias by electro deposition for then make sure to have the electrical contact (Fig.5 & 6).

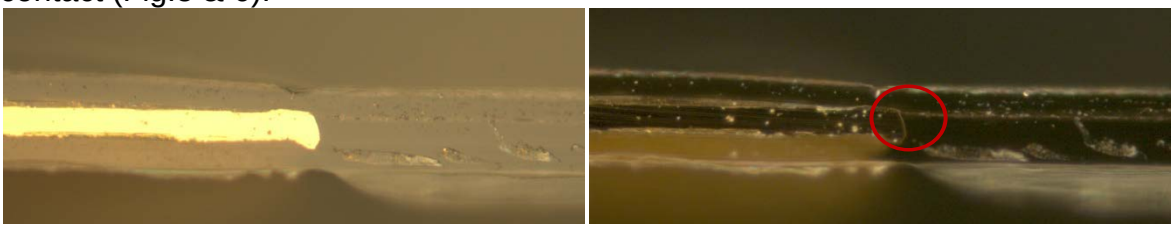


Fig.5 & 6: pictures of 9µm gold vias and the metallization line on the top

The release of the structure is done by peeling naturally the layer with a knife for the PI2611 and by dipping in HF solution for HD4110. We measure with a mechanical profilometer a residual constraint of 0.5MPa on 25µm PI2611 and a little more for the HD4110 which is quite negligible.
Then, we can take the electrical contact on top or bottom (Fig.7) by glue, paste deposition or by wire bonding. Components can be mounted on top or bottom by the same way (Fig.8 & 9).

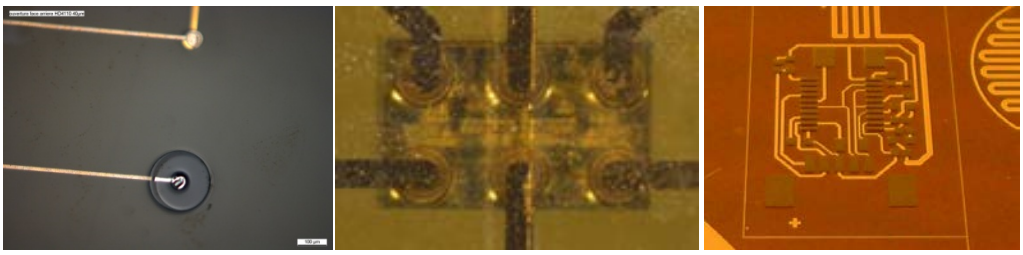


Fig.7,8,9: Via opening on bottom; Back view of a silicon component mounted with BGA; view of a screen printing SAC deposition on polyimide.

Conclusion

We present here a simple technique for the realization of a flexible substrate ranging from few microns to hundred microns thickness, not deformed, keeping specificities of the original design. This is being able to be done by using the microelectronics equipments. It's possible to use alternative technologies (screen printing, inkjet, roll to roll) to do it. Actually, we work on a process to make the vias on the polyimide by screen printing and by the same way to fill them with conductive glue.

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