Methodology for accurate diagnostic of defects in III-N HEMT technologies

non-destructive and destructive experimental tools - electrical and T-CAD models

Invited paper

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***Abstract*—III-V wide bandgap disruptive technology is firmly positioned as a leader for high power segments operating at high frequency or under switching mode. Still, it is needed to investigate these transistors to push the maturity towards higher levels and to address elevated junction temperatures. Concerning analog RF applications, more than two decades of studies lay the main technological process basis for both obtaining improved RF performances and reliability. However, if failure signatures and their associated defects are now issues likely to be understood as individual problems, the global failure behavior still poses challenges to overcome. This paper is a contribution to the failure analysis studies on GaN technologies by providing a methodology for ensuring the validity of the stress analysis, to the accurate identification of the involved defects; this procedure is suitable even for a single stress test campaign, when usually several accelerated life tests are needed to separate concurrently proceeding effects. This methodology is based on the use of destructive and non-destructive characterization techniques, as well as electrical modelling. Key degradation processes are highlighted from different feedback studies, still considering the need of a secure procedure to avoid any misunderstanding about the origin of the tracked DC or RF variation of the devices under test.**

Keywords—GaN HEMT; reliability; stress; failure analysis methodology; transient characterization; frequency characterization; LFN; stress workbench; T-CAD model; Large-signal model

I. INTRODUCTION

III-V wide bandgap devices are now reaching a Technology Readiness Level (TRL) sufficiently high to address various applications; the principle market segments targeted by GaN High Electron Mobility Transistors (HEMT) for high-power, high-frequency transistors are wireless infrastructure (base stations and backhaul), defense and military applications (radar, jamming, counter-measures, guided weapons, etc.), broadcast and communication satellites (SatCom). From these different markets, it can be distinguished categories of applications that feature the same trends regarding the reliability needs, the cost and other performance, size or legacy considerations. For the foundries and brokers, to win the innovation race in terms of performance cannot be dissociated from providing the customers with highly reliable devices. More than 20 industrial laboratories are engaged in the market of GaN HEMT for RF applications, and a summary of long-term accelerated tests on Nitride HEMT carried out by some of these technology brokers can be found in [1]. During the last decades, channel temperature junction has been improved as shown by G. David in its survey of the literature (improvement of MTTF by more than 10^6 factor from 2007 to 2014 @ 150°C, 175°C and 200°C [2]). These advances have been obtained thanks to sustained efforts on technological improvement, accompanied by better understanding of the failure signature in GaN devices. But the complexity of the defects root causes in the devices is still to be understood to push these GaN technologies close to their theoretical limits. Parameters involved in the reliability of the devices are related to the design, the processing and the packaging steps. A large variation on the nature of devices is found in the literature (wafer or die level, small or large devices, packaged or naked die). According to the low or high value of TRL, the studies will more concern wafer level and naked die during process improvement phases, whereas packaged devices will be more representative for qualification steps. From the abundant literature concerning this challenging domain of study, a large variety of papers is dedicated to specific failure analysis studies in GaN devices, some of them propose new analysis tools, present a methodology for failure analysis [3][4][5][6][7] or propose a general overview concerning the reliability in GaN devices [8][9][10]. Usually, the identification of a complex failure signature is achieved by performing various stress campaigns under changing conditions to separate effects of mechanisms proceeding concurrently to a failure signature. This approach is time-consuming and is not always applicable for studies featuring only one batch of stressed samples. This last study case represents a situation where it is necessary to get numerous parameters from a unique equation – which is impossible if using a single analysis tool.

We propose in this paper a methodology suitable to identify various defects revealed under multi-factor stressing conditions (i.e. DC biasing with temperature and pulsed/CW radiofrequency signal). As stated previously, a large set of experimental workbenches and dedicated models are needed to reach this objective of fine and secured analysis of the physical failure mechanisms, and their links. Lastly, a single stress experience will not allow to extract (thermal) activation

energies, and at least three stress campaigns at different temperatures will be needed to extract such parameter from Arrhenius plot. It must be noticed that Arrhenius plots are not considered to accurately account for GaN technologies reliability predictions (even by using scaling factors [4]), and a better knowledge of the concurring defects is much prone to define security operating areas for circuit design.

The proposed methodology (and associated experimental tools or stress workbenches) has been attested and improved using several foundries, and over a large set of DC or RF stresses. Fig.1 summarizes the structure on which the methodology is based; it makes use of experimental analysis and of modelling techniques targeting the final diagnostic on failure root mechanisms.

The paper is divided in 5 sections: after this introductive first section, the second section presents the largely accepted stress conditions and tests, and the experimental workbench developed in our laboratory. In the third section, the main and more efficient experimental diagnostic tools are presented, with a highlight on their complementarity. Then section four concerns the development of electrical models (dynamic large signal models for circuit design and reliability analysis, and T-CAD models for physical acceptability of the diagnostic). The two last sections summarize the main achieved results and conclude about the need to use a robust methodology for reliability studies of III-N technologies.

II. Stress Conditions and Tests

A. *Main stress tests towards process improvement and process qualification*

According to the final objectives (electrical operating mode, harsh environment, …), reliability tests are needed to find out the first order degradation signature and related mechanism to be solved. Reliability studies aim to make the technology pass the lifetime requirements. When passing a critical lifetime requirement (usually 10 years of operation), then junction temperature requirement can be pushed towards higher limits. So thermal stresses are largely used during life tests. Usually completed tests by GaN companies according to widely accepted standardized stresses are listed below:

-DC life tests (DCLT): HTRB (High Temperature Reverse Bias), HTOL (High Temperature Operating Life, Fig. 2) and I_{DQ}-I_{GQ} (variations of drain or gate quiescent current at ambient temperature under very deep AB or AB operation class) can be operated at different constant V_{DS} voltages, or by step variation. Different parameters are tuned during the stress period (biasing drain current $I_{Dquiescent}$, saturation drain current I_{DSS}, threshold voltage V_{th}, leakage currents $I_{G\text{-}leak}$-$I_{D\text{-}leak}$, static transconductance g_m, drain and gate voltages). Stopping condition of the stress is usually given at 10% variation of $I_{Dquiescent}$, or according to a limitation of leakage current before destruction of the gate.

-RF life tests (RFLT): CW at different output power (compression) is convenient to capitalize time variation of the dynamic and static parameters over long time. Step stresses are used to assess the aptitude of the devices to sustain critical RF levels for rugged applications.

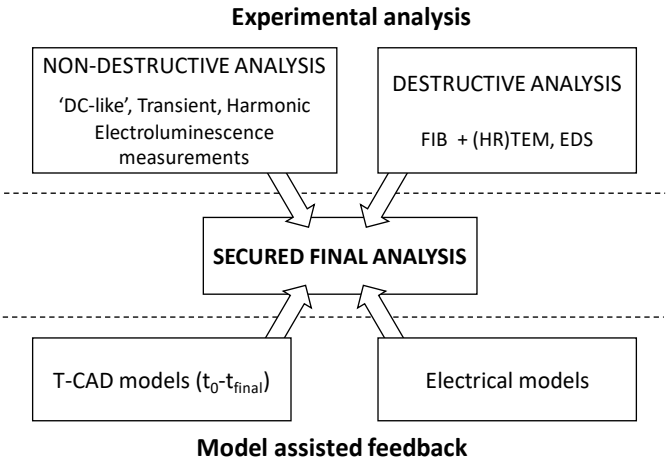

Fig. 1. cross analysis of non-destructive and destructive analysis with electrical models for secured stress analysis. Characterizations are performed on virgin (or initial measurement) and stressed (or final measurement) devices, with possible intermediate measurements. Physical origins of the defect can be assessed, and limits of operation can be defined closely related to the stress conditions.

-Additive stresses can also be achieved under given ambient conditions (moisture, radiation, mechanical vibration & acceleration, etc…).

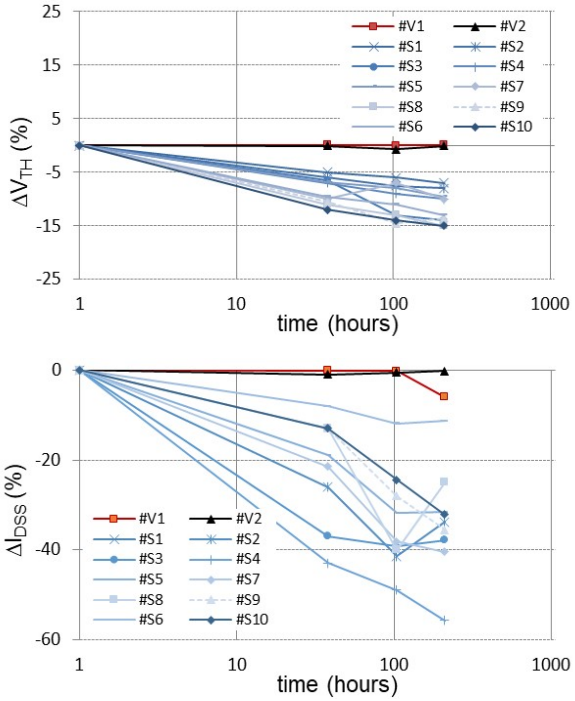

Fig. 2. Example of HTOL stress on a sample of ten 0.25x8x125µm HEMT devices #S_i (two virgin devices #V_j). Graphs report on the threshold voltage V_{TH} and on the saturation drain current I_{DSS} drifts during 210 hours of stress.

Each DC life test is time consuming, and several tests are needed to evidence one degradation (acceleration) parameter. RF tests are closer to the application context but more difficult to analyze because of the conjugated effects; scaling factors are then used on the bases of DC tests, but at the expense of longer analysis period (if 1000 h per single test is performed, over 3 DC

+ 1 RF tests are needed at least, thus corresponding to half a year if cumulated).

B. RF-Thermal experimental stress workbench

For specific application purposes, it can be developed appropriate stress tests. For example, robustness of rugged low noise amplifiers (LNA) versus jamming signals for radar applications needs to study the behavior of the devices/circuits versus RF step stresses (different tests, recovering periods, removing charges procedures). RF stresses are one of the harshest tests as all the DC-thermal-RF swings make the puzzle more difficult with more parameters to consider together. More than ever, setting an appropriate experimental procedure to discriminate between some (potentially) degrading parameters is needed.

An evolving RF stress workbench with programmable thermal pattern of the oven has been developed that allows to track static quiescent conditions of the devices under test, dynamic powers at the input/output of the devices (@ RF stress frequency between 0.1 GHz to 40 GHz), S-parameters (removing RF-stress during [S] parameters measurement), fundamental P_{out}-P_{in} plot. Noise Figure measurement acquisition is under development for studies of LNAs under RF/thermal stress. It is a major issue during RF stresses to keep constant or to get feedback over stability of all the circuitry of the stress workbench, out of the DUTs. This is why temperature of the oven and that of the ambient room are also monitored (+/- 0.1°C measurement accuracy). More critical, as four different channels are available in our configuration, three channels are devoted to DUTs, and a control channel is saved to secure the analysis with potential drifts from the driver module (synthesizer and power amplifier) (Fig.3).

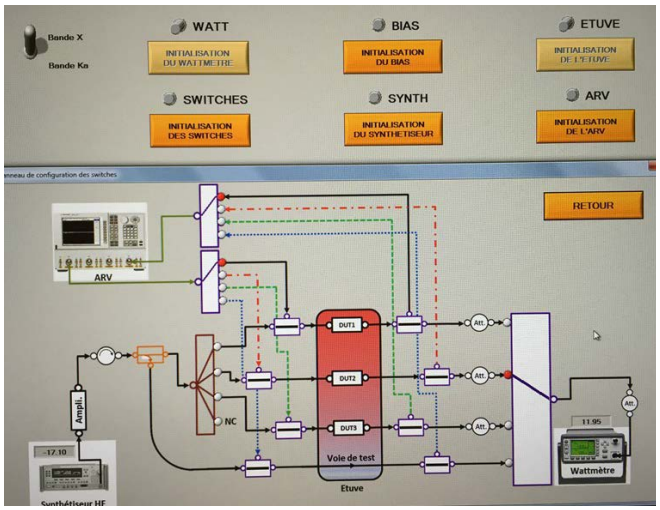

Fig. 3. Screenshot of the fully-automated workbench used for RF/thermal stresses using step stresses or CW signals ranging from 0.1 GHz to 40 GHz. Thermal cycles slopes are considered for temperature stabilization of the devices (from -40 to +150°C). Vector Network Analyser collects [S] parameters with individual calibration set for each channel at intermediate times (very small variation of the calibration during hot/cold cycles and over a large period of use, less than 0.12dB insertion losses over 2 weeks).

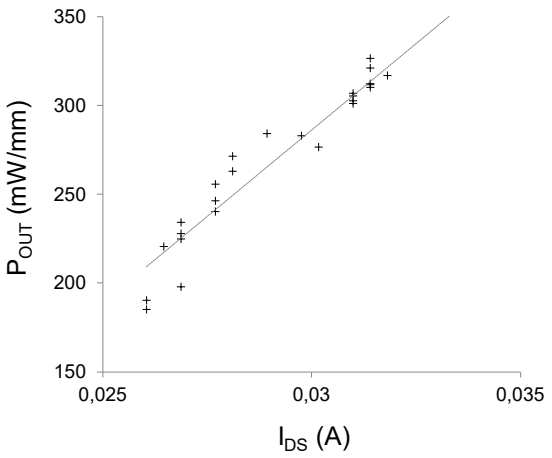

Fig. 4. Correlation between I_{DS} static current and P_{OUT} normalized output power @10GHz during 2400 hours of RF=10 GHz stress at 3dB power compression. HEMT device under test is 0.25x2x75µm²

Fig. 4 presents the correlated variation of the RF output power with the static drain current, and Fig. 5 plots the P_{OUT}-P_{IN} before and after stress (intermediate plots are also available). These data are used together with other characterization and simulation tools presented in the next sections to complete the map for understanding the underlying fine mechanisms of the stress. Here, accumulation of positive charges under the gate change the intrinsic bias of the 2DEG, and modulate the carriers density n_i (thus I_{DS}). The dynamic gain improves (dBS_{21}) and the P_{1dB} compression point decreases as revealed in Fig. 5.

To the three questions addressed by industrial founders for a process qualification (what happens? when does it happen? where does it take place?), two more questions must be discussed additionally (why and how do the defects reveal?). These last questions usually need specific experimental workbenches available in academic laboratories. The next section shows some experimental setups used for failure analysis studies, with objective to answer to the previous set of questions.

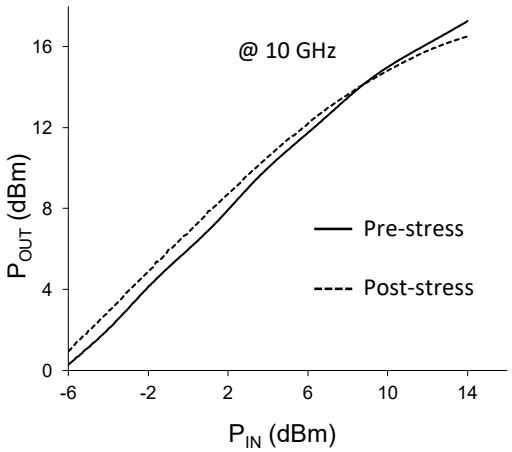

Fig. 5. P_{out}-P_{in} plot for a typical 0.25x2x75µm² AlGaN/GaN HEMT device before (line) and after (dashed) the application of RF stress for 2400 hours @ 10 GHz under 3dB compression point.

III. Different crossed experimental techniques

GaN High Electron Mobility Transistors are obviously robust wide bandgap devices, but they are also sensitive to electrical charges, depending on local or global thermal states, on electrical fields and mechanical strains due to spontaneous and piezoelectrical charges at different interfaces of the layers. Related defects and resultant failure analysis can be revealed with experimental tools, directly by targeting the active area (destructive tools) or by deduction from external measurements (non-destructive tools).

A. Non-destructive techniques before/during/after stress

Experimental tools allowing electrical (transient or harmonic) characterizations are attractive because the device under test is not supposed to evolve during the characterization. Then consequent sets of data can be compared at different stress times for fine analysis or modelling (versus electrical models or for T-CAD model instruction). However, the measurement is mainly extrinsic to the invoked zone where the failure mechanism takes place, and a rigorous procedure associated to the experimental setup is needed to lower the speculative aspects of the resulting outcomes. First, it has to be considered seriously that non-destructive measurement technique does not necessarily mean non-invasive measurement. Test conditions can interact with some defects according to the setup of the workbench. Fig. 6 illustrates the sensitivity of a new generation InAlN/GaN HEMT device relatively to the acquisition time instructed for a signal analyzer during so-called 'static' or 'DC' output I_{DS}-V_{DS} (and transfer I_{DS}-V_{GS}) characteristics.

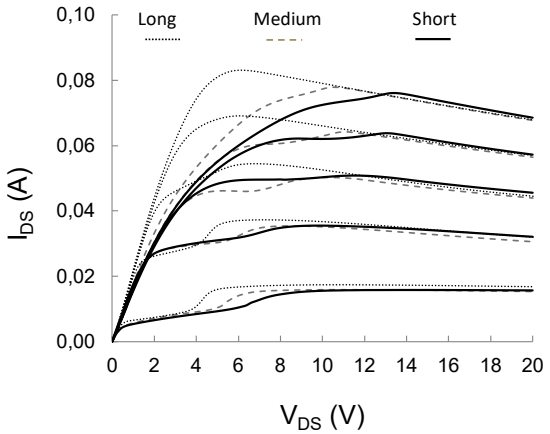

Fig. 6. Illustration of invasive DC-measurement on output characteristics of a 0.25x2x50 µm² HEMT (Measurement performed on a not yet mature InAlN/GaN HEMT process). I-V characteristics are given for different acquisition time configurations (acquisition time per data point - Short=640µs / Medium=20ms / Long=320ms) using 4156C Keysight Signal Analyser.

When such variation occurs in output 'static' characteristics, then electrical models using short or medium measurement configurations are erroneous due to those side effects, considered as the manifestation of memory effects. Even during S-parameters measurement, frequency dispersion can appear at frequencies well below the starting frequency conditions (usually 40 MHz). In the case of DC or S-parameters variation according to measurement conditions, resultant models will be inappropriate for analysis before, during or after the application of a stress (and inappropriate of course for circuit design).

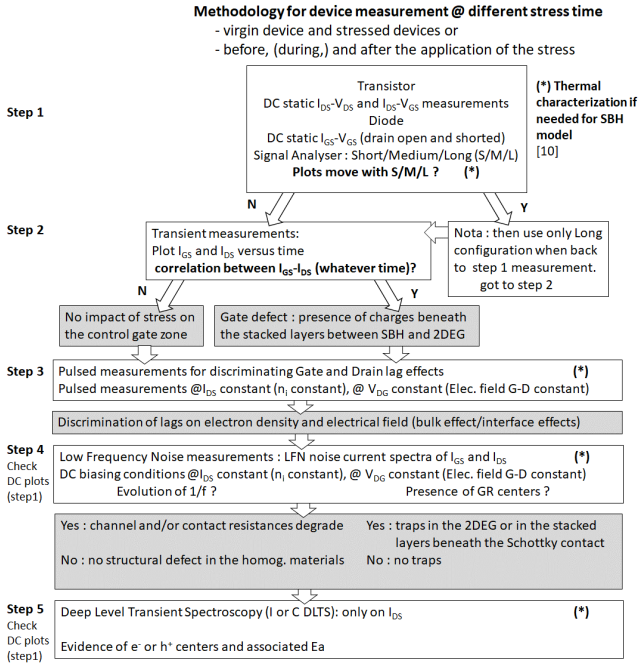

Fig. 7. Measurement methodology using transient and harmonic measurements to reveal defects in the HEMT. Comparison between initial/final measurements defines the location and the origin of the defects.

The methodology used for each characterization before and after the application of the stress is depicted in Fig. 7. In this procedure, data from the stress file (i.e. P_{out} versus time, DC currents versus time, [S] parameters) are analyzed together with initial and final set of measurements proposed in Fig. 7. It is also possible to partition the stress campaign to have more intermediate results.

- DC measurements stand as reference measurement to ensure the integrity of the electrical signatures of the DUTs during the procedure of Fig. 7. If these characteristics change, then fine analysis between step 1 and step 5 is nonsense (step 1, step 4, step 5).
- Transient measurements give a first insight about short, medium or long memory effects or trap related effects. The correlation between I_{GS}(time) and I_{DS}(time) gives a first order information about the common nature of the defect charges under the gate [10] (step 2). A procedure is proposed in [11] for lag analysis on gate and drain currents using pulsed measurements (step 3).
- Low Frequency Noise spectra (from 1 Hz to 1 MHz) are known to be very sensitive to the quality of the material and to the presence on defects on the path where the current flows (gate S_{IG} and drain S_{ID} noise current spectral densities). Measurements under different biasing conditions permit the identification of DC voltage or current sensitivity of traps (Generation Recombination centers if present in the measured spectra) (step 4). From the literature, it is often illustrated that S_{ID} remains constant before and after the application of a stress, despite numerous GR distributed over the frequency range; this means that defects are present (and can vary with bias), but are not necessarily impacted by stress. On the contrary, S_{IG} is very sensitive to charge or trap evolutions and

can stand as a great marker of defects under the Schottky command [11][12].

- Capacitance or current Deep Level Transient Spectroscopy (C- or I-DLTS) measurements are performed over a temperature range of 90 K -450 K (step 5). Activation energy and section of the traps are extracted and compared with the GR centers from LFN measurements in step 4 [13].

Other characterization tools have been used successfully (not identified in Fig. 7), but in total agreement with the intended goal of defect evidence and characterization. For instance photo Emission Microscopy (EMMI), Optical Beam Induced Resistance Change (OBIRCH) technique [14], electroluminescence, or other athermal A-DCTS techniques [15] and C-V measurements are providing the users with key complementary clues.

B. Destructive techniques (before/) after stress

Non-destructive techniques can also be considered as speculative because of the indirect proof of a failure mechanism (especially when different defect mechanisms are engaged). Destructive technique focus on the active part of the defect (according to the difficulty to find out the related location). But if the manifestation of defects can be proved by direct location of structural/chemical degradation in a stressed device (compared to a virgin device), a question still rises from such an approach: does this defect play a role in the electrical signature of the device? Statistic approach also strengthens the conclusions from these studies, but definitely it will not be easy to check intermediate steps during stress periods; this would imply a large number of (homogeneous) samples for each stress, removing few devices at given moment of the stress. Then the correlation of studies as proposed in Fig. 1 reduces the risk of speculative answers by crossing independent issues.

Very sensitive characterization tools such as HAADF STEM with atomic number contrast in the stacked layers, TEM lamella after gate foot removing, EDX spectroscopy analysis have been used in [16] with T-CAD models and electrical measurements to differentiate defects origins responsible of various failure signatures.

IV. MODELS FOR FAILURE ANALYSIS

From electrical (large signal) measurements, it is possible to develop non-linear models; the availability of such a model with failure signatures associated is useful for circuit design. Design of a circuit at initial t_0 and also considering parametric shifts at final t_{stress} can help the designer for topology optimization. Here, T-CAD models (using Sentaurus-Synopsys) are more under concern as the paper deals with failure analysis. Physical modeling of degradation mechanisms thanks to 2D simulations of the active device helps to understand III-N HEMT failure modes; the instruction of physical parameters in a specific region of the model gives helpful feedback on experimental results.

Effects of charges and traps in terms of nature, location, energy level, density, section, (bulk, interface, under the gated or ungated zones G-S and G-D) can be evaluated on the output I_{DS}-V_{DS} and transfer characteristics I_{DS}-V_{GS} (G_m-V_{GS}) [16], and on leakage currents I_{GS}-V_{GS} (diode and transistor mode).

After an exhaustive study concerning the way to instruct the defects and to simulate the parameters, the impact of donors or acceptors in the bulk and at the different interfaces, one can dispose of a large variety of parameters, each associated to a failure signature. Then, regarding the experimental plots, it is possible to tune such T-CAD model to match the measurement in a realistic way.

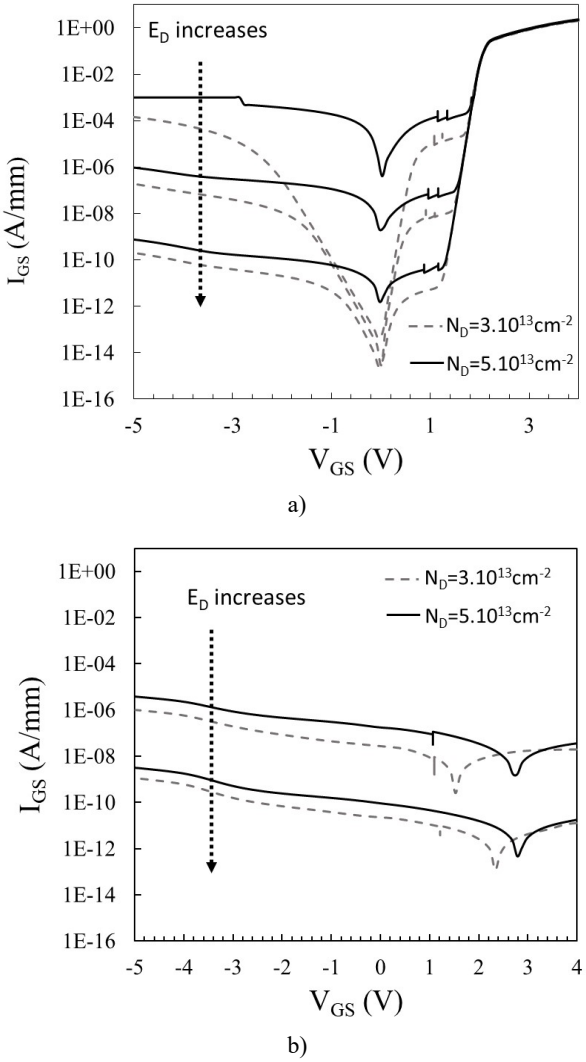

Fig. 8. Simulated leakage I_{GS}-V_{GS} characteristic (V_{DS}=0V for figure a, and V_{DS}=8V for figure b), versus different donor activation energies and concentrations. Energies E_D are situated at (0.1eV figure a), 0.3eV and 0.5eV below the conduction band, with donor concentration n_D at $3.10^{13}cm^{-2}$ and $5.10^{13}cm^{-2}$.

Donor-like centers in the bulk account for I_{GS}-V_{GS} magnitude variation as revealed by some HTRB or HTOL stresses. It is likely to suppose that, for a fixed activation energy of the donor-like centers, only the concentration increases with the application of the stress, as reported in Fig. 8 a) (donor located at the SiN/GaN cap layer interface); the rapid increase of the leakage current from part of this inversion voltage, featuring a plateau, is reported in many papers [17][18], and even concerns GaN-based LEDs [19]. Furthermore, Fig. 8 b) illustrates how the inversion voltage shifts largely considering

different donor concentrations, and for activation energies situated 0.3eV below the conduction band E_C, in transistor mode (no variation of V_{th} versus n_D is revealed for 'deep centers' as reported for E_D=0.5eV below E_C). The closer the activation energy to the conduction band, the more pronounced the variation shift of the inversion voltage. Depending on the epitaxial and passivation process, the simulation can fit to account for specific electrical signatures.

V. Global Overview Concerning Failure Analysis Results From Previous Studies on GaN HEMTs

From the proposed set of experimental and simulation tools, we are able to reduce the number of speculative assumptions concerning the possibly involved mechanisms from a given file of stress. The detection and the location of charges at different interfaces under the gate and between gate-source and gate-drain regions, the possible transient correlation between gate and drain currents related to time-varying charges under the gate, and the analysis of the gate leakage current behaviors versus temperature are some of the outcomes from such previous works. As one of the dominant failure mode of GaN HEMT devices relates to a gradual RF output power degradation (wear-out), generally correlated with the (recoverable) decrease in the drain current (current collapse), studies have been focused on the impact of RF power. The role of RF-activated traps and charges has been evidenced on the degradation mechanism for different compression levels. From some studies summed up in this paper, we are able to discriminate between defects in the channel (usually not stress dependent) and defects activated by stress in the outer zones of the main electron flow (from source to drain), featuring recoverable or permanent effects. These techniques have made it possible to improve different academic and industrial GaN processes.

VI. CONCLUSION

The optimization of a GaN technological process concerns the understanding and the mastering of failure mechanisms, still considering a roadmap towards increased frequency and power added efficiency. Failure analysis for RF stresses are among the more difficult to achieve as many parameters are involved in the different RF and DC electrical signatures before and after stress. A set of DC/thermal/RF stresses is usually needed for the identification of such degradation processes, which represent long study times. In this paper are identified a set of (non) destructive measurement techniques that can be confronted with T-CAD simulations to secure the failure analysis as presented in Fig. 1. It is then possible to identify root physical degradation defects involved in many different (RF or DC) electrical signatures from a single RF life test. Obviously, this methodology does not allow the extraction of activation energies needed to get the mean time to failure; it can however be easily reached if used with three different temperature life tests.

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