



**HAL**  
open science

## Optimisation de la diode à Superjonction à tranchées profondes pour des applications à 600V

Sylvain Noblecourt, Josiane Tasselli, Frédéric Morancho, Karine Isoird,  
Patrick Austin, Pascal Dubreuil, Aurélie Lecestre

### ► To cite this version:

Sylvain Noblecourt, Josiane Tasselli, Frédéric Morancho, Karine Isoird, Patrick Austin, et al.. Optimisation de la diode à Superjonction à tranchées profondes pour des applications à 600V. *European Journal of Electrical Engineering*, 2014, 17 (5-6), pp.345-361. 10.3166/ejee.17.345-361 . hal-01955633

**HAL Id: hal-01955633**

**<https://laas.hal.science/hal-01955633>**

Submitted on 14 Dec 2018

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

---

# Design and realization of Deep Trench SuperJunction Diode for 600V applications

Sylvain NOBLECOURT<sup>1,2</sup>, Josiane TASSELLI<sup>1,3</sup>, Frédéric MORANCHO<sup>1,2</sup>, Karine ISOIRD<sup>1,2</sup>, Patrick AUSTIN<sup>1,2</sup>, Pascal DUBREUIL<sup>1,3</sup>, Aurélie LECESTRE<sup>1,3</sup>

1. CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France

2. Univ de Toulouse, UPS, LAAS, F-31400 Toulouse, France

3. Univ de Toulouse, LAAS, F-31400 Toulouse, France

---

*ABSTRACT – The purpose of this paper is to present the Deep Trench SuperJunction Diode (DT-SJDiode) optimization and realization with a 600V breakdown voltage. We present technological and geometrical parameters influences on the breakdown voltage with simulations performed with Sentaurus TCAD. Previous works allowed to validate some critical technological process steps and to create a technological process for 1200V breakdown voltage applications. The main point here is to optimize those process steps (trench verticality, termination fulfilling...), which have an important influence on the electrical properties, in order to fabricate a 600V breakdown voltage DT-SJDiode.*

*RESUME - L'objectif de ce papier est de présenter l'optimisation et la réalisation d'une diode à superjonction et à tranchées profondes et de sa terminaison (DT-SJDiode) pouvant tenir des tensions de 600 V à l'état bloqué. Nous étudierons l'influence des paramètres technologiques et géométriques sur la tenue en tension à partir de simulations effectuées sous Sentaurus TCAD. Des travaux précédents ont permis de valider certaines étapes technologiques et de dégager un procédé de fabrication pour des applications à 1200V. Il s'agit ici d'optimiser ces différentes étapes qui influent sur les paramètres électriques (verticalité des tranchées, remplissage des tranchées de terminaison de jonction, ...) pour des applications à 600V.*

*KEYWORD—Superjunction Diode—Deep Trench Termination—BenzoCycloButene*

*Mots-clés—Diode à Superjonction—Terminaison à tranchées profondes—BenzoCycloButène*

---

## Extended Abstract

New technological ways allowing the realization of deep trench Superjunction devices (diodes or MOS transistors) with a deep trench termination are investigated. The aim of this work is to propose an alternative to conventional MOSFETs in high

voltage range (600 V and above): the major challenge is to find the best trade-off between the two main parameters characteristics of these structures: specific on-resistance / breakdown voltage. We developed a technology based on a single N-epitaxial layer (thus reducing the realization cost) and the use of BCB filled, wide and deep trenches associated to boron doping on the trenches sidewalls. Previous works have demonstrated the feasibility of such junction termination and have led to the fabrication of a 1200 V Deep Trench Termination Diode (DT<sup>2</sup>-Diode). We chose to validate our termination technology by fabricating a Deep trench Superjunction Diode (DT-SJDiode) for 600V applications. By means of Sentaurus TCAD 2D-simulations, we have first determined the optimal physical and geometrical parameters leading to a best “Breakdown voltage/on-state resistance” trade-off. For example, for a N- epitaxial region doping concentration of  $3 \times 10^{15} \text{ cm}^{-3}$ , a distance between two central trenches of 8,5  $\mu\text{m}$ , and a trench termination width of 40  $\mu\text{m}$  in particular, the breakdown voltage is 595 V and the specific on-state resistance is 126  $\mu\Omega.\text{cm}^2$ . We presented technological results focusing on the more critical points: the control of deep trenches verticality by Deep Reactive Ion Etching technique, according to the Bosch process, and the trench filling with dielectric. We have studied the influence of SF<sub>6</sub> etch and C<sub>4</sub>F<sub>8</sub> passivation times on resulting trench verticality: the best anisotropy for 6 $\mu\text{m}$  wide central trenches and 40  $\mu\text{m}$  wide termination trenches is obtained for the couple SF<sub>6</sub> (2 s)/ C<sub>4</sub>F<sub>8</sub> (3.5 s). A thermal oxidation after the etch step allows to reduce the size of the scallops that appear on the trenches sidewalls and characteristics of the Bosch process (alternation of etch and passivation steps): the related peak-to-valley distance is lowered from 100 nm to 50 nm. Finally we have successfully filled deep and wide trenches by optimizing the BCB spin-coating parameters, the high viscosity of this material rendering difficult its spreading all over the wafer. We found that a dispensing rotation speed down to 100 rpm and an implementation of two 10 min rest steps improve BCB spreading and its flowing along the trenches. The BCB excess removing by reactive ion etching is under study: first encouraging results give an etch rate of 0.75  $\mu\text{m}.\text{min}^{-1}$  with a SF<sub>6</sub>/O<sub>2</sub> gas mixture.

## 1. Introduction

Today, up to 600 V-breakdown voltage, the main IGBT competitor is the MOSFET. Indeed, the MOSFET exhibits many interesting properties for power applications: high switching speed, high input impedance and thermal stability. However, in high voltage range (600 V and above), conventional MOSFETs are limited by their very high specific on-resistance and, therefore, their high on-state voltage drop, which induces more on-state losses, compared to bipolar devices. This specific on-state resistance is inversely proportional to the doping concentration of the drift region, which must be low enough to sustain the off-state voltage: to find the best trade-off between these two parameters (specific on-resistance / breakdown voltage) is one of the major challenges in this voltage range.

For this reason, several innovative unipolar structures have been proposed: the common idea is the structural modification of the drift region in order to overcome

the theoretical limit of the 'specific on-resistance / breakdown voltage' trade-off of conventional unipolar power devices. The main concept is the well-known superjunction, which is implemented in power MOSFETs for years. It is based on the use of several sequences of 'N-epitaxy then P-implantation' (or opposite) in order to realize the drift region, which is a vertical alternation of N and P columns. This technology was chosen in particular by Infineon for the realization of COOLMOS™ transistors (Lorenz et al., 1999) and by STMicroelectronics for the realization of MDMESH™ devices (Sagio et al., 2000). However, the manufacturing cost of this technology can be very high because the process requires a significant number of masks. The breakdown voltage of these superjunction devices is also limited by the terminations (device peripheries) which are less effective when the drift region is strongly doped (which is the case and the interest of superjunction devices).

In this study, we propose new technological ways allowing the realization of deep trench superjunction devices (diodes and MOS transistors) with their appropriate termination (a deep trench termination) without using a multi-epitaxy process. Our objective is to set up a technology with a single epitaxial layer and the use of dielectric-filled, wide and deep trenches associated to boron doping on the trench sidewalls. Before realizing a superjunction MOSFET, we chose to validate our technological choice by first fabricating a Deep Trench superjunction Diode (DT-SJDiode) for 600V applications. The main challenges for the deep trench technology are the trenches verticality to ensure a perfect charges balance, the implantation uniformity on the trenches sidewalls and the filling of the trenches with a dielectric.

The design and optimization of this DT-SJDiode are first done by means of Sentaurus TCAD 2D-simulations. The objective is to determine the optimal physical and geometrical parameters allowing the achievement of the best 'Breakdown voltage/on- state resistance' trade-off. Then, we present the first technological results focusing on the critical points of the developed technology, i.e control of the deep trenches verticality, P-doping on sidewalls and dielectric trench-filling.

## 2. Definitions and principles

### 2.1. Structure description

A cross-sectional view of the proposed DT-SJDiode is represented **Figure 1**. It is based on elementary cells allowing the implementation of the superjunction principle (Fujihira, 1997), i.e. an alternation of N and P regions in the volume. To ensure the maximal breakdown voltage, the superjunction is protected in periphery of the active zone by means of a guarding technique developed in the laboratory (Theolier et al., 2009). We use a dielectric filled wide and deep trench with a field plate on top. The use of deep trenches allows to avoid a multi-epitaxy technology. The P<sup>+</sup> region is realized on the trench sidewalls from boron doping by Plasma-

Immersion Ionic Implantation (PIII) (Nizou et al., 2006). The dielectric is the BCB (Cyclotene 4026-46) (Dow Chemical Company, 2005) whose electrical parameters (critical field of  $5.3 \text{ MV}\cdot\text{cm}^{-1}$  and dielectric constant of 2.65) allow to ensure the efficiency of the junction termination.

The parameters which are studied for the structure optimization are: the trench depth  $D_T$ , the implanted boron dose to obtain  $P^+$  regions, the doping concentration of the  $N^-$  epitaxial zone, as well as the spacing  $W_N$  between two nearby central trenches. The  $N^-$  doping concentration is fixed at  $3.10^{15} \text{ cm}^{-3}$ : indeed, previous studies (Theolier, 2008) have shown that a higher concentration will increase the difficulty of the implantation step.

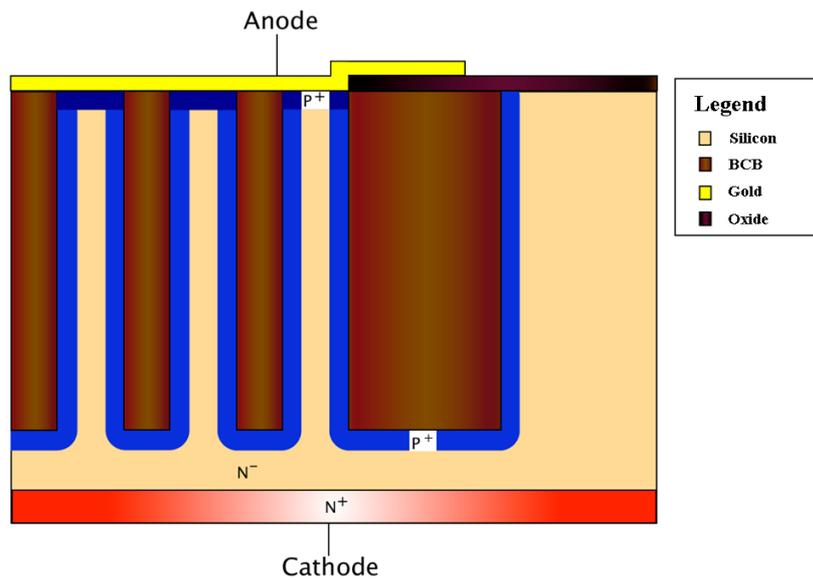


Figure 1: Schematic cross-section of the DT-SJ Diode

## 2.2. Study of the 'breakdown voltage/on-state resistance' trade-off

All the physical and geometrical parameters influence both the breakdown voltage and on-state resistance. To obtain the best trade-off, we first have optimized the specific on-state resistance in order to study its impact on the breakdown voltage. To do so, we have simulated a single elementary cell, the central trenches width  $W_T$  and the  $P^+$  zone width  $W_P$  being respectively fixed to  $6 \mu\text{m}$  and  $1 \mu\text{m}$ .

The on-state resistance is mainly due to the drift resistance, which is the resistance of the  $N^-$  epitaxial layer. For a given doping concentration  $N_D$ , it can be assimilated to a simple bar of  $N^-$  type silicon of  $W_N$ -width and  $D_{EPI}$ -length or the trench depth  $D_T$ , assuming that:  $D_{EPI} = D_T + k$ ,  $k$  being the distance between the bottom of the trenches and the  $N^+$  substrate ( $k$  is kept constant in our study:

$k = 3 \mu\text{m}$ ). **Figure 2** shows the variations of the specific on-state resistance according to  $D_T$  for various values of  $W_N$  for a doping concentration  $N_D$  of  $3.10^{15} \text{ cm}^{-3}$ . A decrease in  $D_T$  or an increase in  $W_N$  leads naturally to a decrease in the specific resistance.

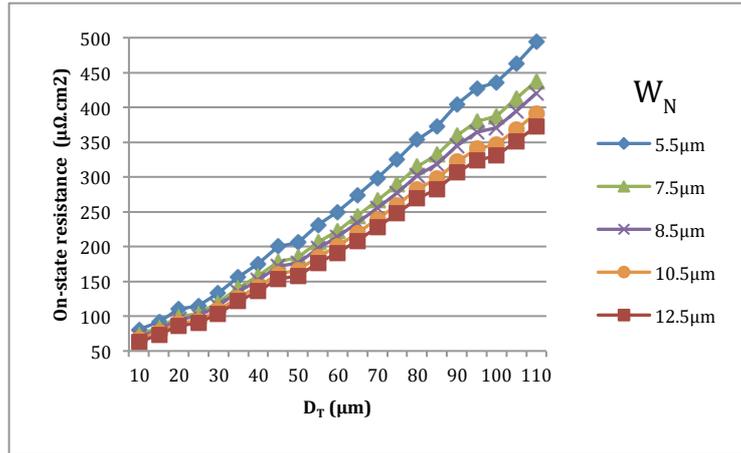


Figure 2: Simulated specific on-state resistance variations of an elementary cell as a function of trench depth  $D_T$  for various intercellular lengths  $W_N$ . The  $N$  epitaxial layer doping concentration ( $N_D$ ) is  $3.10^{15} \text{ cm}^{-3}$ .

For an optimized superjunction,  $D_T$  is the key parameter allowing the adjustment of the desired breakdown voltage: the higher  $D_T$ , the higher the breakdown voltage. **Figure 3** shows the variations of the breakdown voltage according to  $D_T$ .

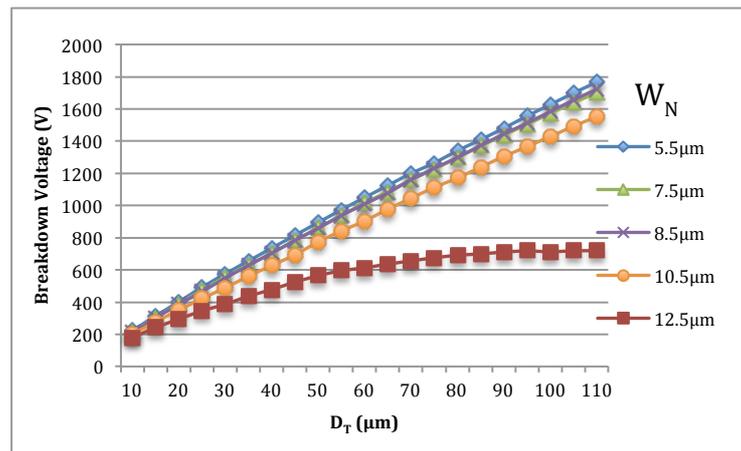


Figure 3: Simulated breakdown voltage variations according to the trench depth  $D_T$  for various values of  $W_N$

The more the depth  $D_T$  increases and the more the depletion region increases thus increasing the electric field circulation and, consequently increasing the breakdown voltage. Unfortunately, the higher is  $D_T$ , the higher is the specific on-state resistance.

By correlating the data of **Figure 2** and **Figure 3**, it is possible to determine the value of  $W_N$  and  $D_T$  which allow to obtain the best 'breakdown voltage/on-state resistance' trade-off. **Figure 4** exhibits, for various desired breakdown voltages, the specific on-state resistance variations with the inter-trench width  $W_N$ . For instance, for a breakdown voltage of 600 V, it can be pointed out that, for  $W_N$  equals to 8.5, the specific on-state resistance presents a minimal value equal to  $126 \mu\Omega.cm^2$ .

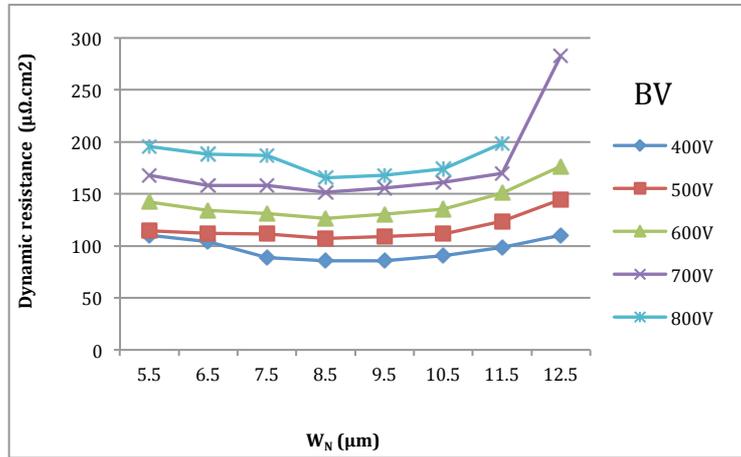


Figure 4: Simulated specific on-state resistance according to  $W_N$  for various values of breakdown voltage

The charge balance between N and P regions is important for the proper functioning of the superjunction and thus for the obtaining of an optimal breakdown voltage. Equation (1) reports this balance in the case of constant doping profiles. Couples  $(W_N ; N_D)$  and  $(W_P ; N_A)$  represent the widths and the doping concentration of N and P regions respectively:

$$W_N \cdot N_D = W_P \cdot N_A \quad (1)$$

An increase in  $W_N$  would naturally lead to a decrease in the specific on-state resistance because of the increase in the conduction section of the current. However, in this case, it would be necessary, as shown in equation (1), to act on the other

parameters. The only constant parameter in our study is the doping concentration  $N_D$  of the  $N^-$  epitaxial layer: the value of  $3 \cdot 10^{15} \text{ cm}^{-3}$  was chosen because this value theoretically allows a reasonable trade-off between electrical performance and technological constraints.

### 3. Optimization of diode parameters

#### 3.1. Influence of the $P^+$ implantation dose

An increase in  $W_N$  implies an increase in the  $P^+$  dose to keep the charge balance. However, the breakdown voltage becomes more sensitive to a charge unbalance compared to the optimal dose: then,  $P^+$  implantation step becomes more critical because some percent of gap compared with the optimal dose makes fall drastically the breakdown voltage (see **Figure 5**).

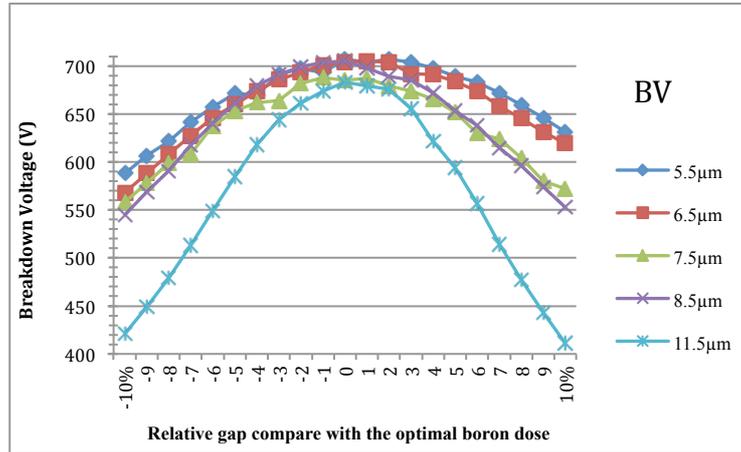


Figure 5: Simulated breakdown voltage variations as a function of the unbalanced boron dose in percent, referring to the optimal dose corresponding to the perfect charge balance, for various  $W_N$  values.

It should be noted that, with our technology, this respect for the physical and geometrical parameters could be valid only if the trench sidewalls are perfectly vertical.

#### 3.2. Optimization of the ' $W_N/D_T$ ' couple

The trench depth  $D_T$  is the parameter allowing the determination of the optimal breakdown voltage. As already shown, the higher  $D_T$ , the higher the breakdown voltage. However, the specific on-state resistance  $R_{ON}$  will increase too. To

overcome this specific on-state resistance increase, two options are possible: to increase the doping concentration  $N_D$  of the  $N^-$  epitaxial layer or to increase the width of the intercellular region  $W_N$ . As already mentioned,  $N_D$  was fixed to  $3 \cdot 10^{15} \text{ cm}^{-3}$ . **Figure 3** shows the impact of the trench depth variations on the breakdown voltage for various values of  $W_N$ . From this figure, it can be deduced the minimal value of the trench depth allowing to obtain the minimal desired breakdown voltage of 600 V. Actually, the breakdown voltage variations are proportional to the trench depth  $D_T$ .

The obvious interest to increase  $W_N$  is to decrease the specific on-state resistance since  $W_N$  is the key parameter related to the conduction section of the device (the conduction section is the ‘silicon / insulator’ ratio). However, the major consequence of this increase in  $W_N$  is the increase in the  $P^+$  implantation dose necessary to ensure the good functioning of the superjunction. Indeed, it is necessary to act on the parameters that are concerned by the charge balance, i.e. the parameters of equation (1). Given that the doping concentration of the epitaxial region  $N_D$  and the implantation depth are fixed, the only degree of freedom stays the implantation dose. Furthermore, beyond  $12 \mu\text{m}$  ( $W_N > 12 \mu\text{m}$ ), the drift region is not anymore able to deplete completely on the horizontal axis. It can be observed that, for  $W_N > 12 \mu\text{m}$ , the slope of the curve is different. The first reason is that it is necessary to have:  $D_T \gg W_N$  so that the principle of superjunction works. Indeed, the junction has to be laterally well depleted before depleting vertically to obtain a breakdown voltage, which is proportional to  $D_T$  and to the critical electrical field  $E_C$ . The second reason is due to the width  $W_P$ , which, even by increasing the P dose, will not be large enough. It would be theoretically possible to increase  $W_P$  but the PIII does not allow to implant deeply thus we are limited by the width  $W_P$ .

### 3.3. Junction termination

For the junction termination, both interesting parameters are the width of the trench termination  $W_{TT}$  and the length of the field plate  $W_{FP}$ , the depth  $D_T$  being above all determined by the constraints of the elementary cell. They influence the breakdown voltage and the distribution and values of the electric field at breakdown.

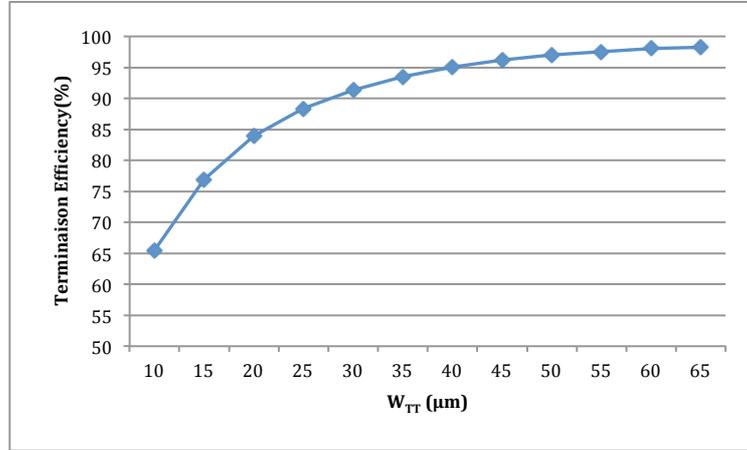


Figure 6: Simulated variations of the trench termination efficiency with  $W_{TT}$  for a 600 V breakdown voltage

The breakdown voltage of the termination depends above all on the parameter  $W_{TT}$ . Simulations of a plane junction using this trench termination were realized in order to determine the efficiency of this termination. **Figure 6** shows that this efficiency reaches 95 % for a trench termination length of 40  $\mu\text{m}$ .

As for the field plate length  $W_{FP}$ , more we increase it, better is the breakdown voltage. On the other hand, by increasing  $W_{FP}$ , the potential lines are tightened between the end of the field plate and the trench sidewalls and thus the electric field reaches its critical value faster. Actually, this is not  $W_{FP}$  that is important but the ' $W_{FP}/W_{TT}$ ' ratio. **Figure 7** shows for instance that, for a ratio equal to 0.65, the electrical field at breakdown is about  $2.4 \times 10^6 \text{ V}\cdot\text{cm}^{-1}$  and the breakdown voltage is close to 700 V. That means that there is a technological margin on the breakdown voltage but also on the electrical field that, as a reminder, does not have to exceed  $3 \text{ MV}\cdot\text{cm}^{-1}$  at the risk of a premature breakdown in the air.

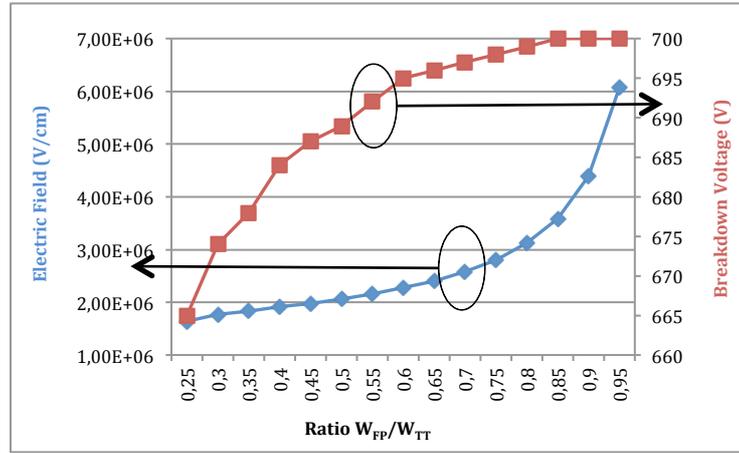


Figure 7: Breakdown voltage and maximal electrical field variations for various values of the ' $W_{FP}/W_{TT}$ ' ratio

### 3.4. Results summary

According to the simulations previously presented, the optimal parameters of the DT-SJDiode were determined for a breakdown voltage of 600 V. Knowing that, at 600 V, the specific on-state resistance is almost similar for a  $W_N$  width between 8.5  $\mu\text{m}$  and 11.5  $\mu\text{m}$  (see Fig. 4), we chose the 8.5  $\mu\text{m}$  value because it allows to minimize the central cell size. According to **Figure 5**, the smallest possible value of P dose was chosen in order to limit breakdown voltage drops, which can occur with a bad precision of the implantation dose.

Table 1. Optimal parameters of the DT-SJDiode

Parameters	Symbols	Optimal values
$N^-$ epitaxial region doping concentration	$N_D$	$3 \times 10^{15} \text{ cm}^{-3}$
Implanted P-dose	DoseP	$1.44 \times 10^{12} \text{ cm}^{-2}$
Distance between two central trenches	$W_N$	8.5 $\mu\text{m}$
P-region width	$W_P$	1 $\mu\text{m}$
Central trench width	$W_T$	6 $\mu\text{m}$
Trench depth	$D_T$	33 $\mu\text{m}$

Trench termination width	$W_{TT}$	40 $\mu\text{m}$
Field plate length	$W_{FP}$	26 $\mu\text{m}$
Breakdown voltage	BV	595 V
Specific on-state resistance	$R_{ON}$	126 $\mu\Omega\cdot\text{cm}^2$

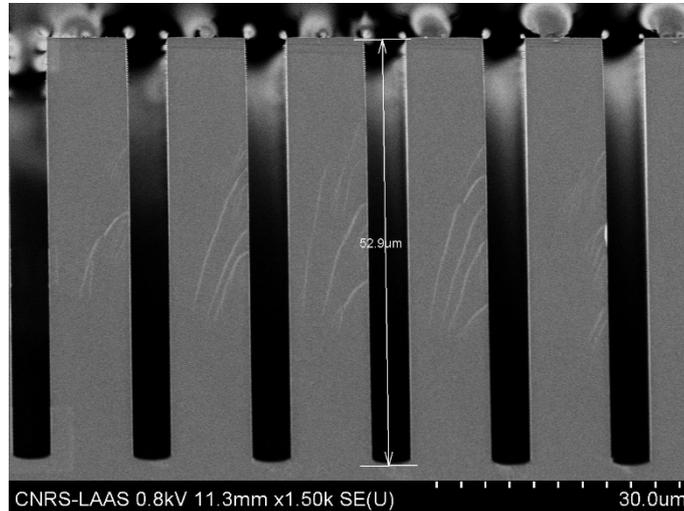
#### 4. Experimental results

The optimization of the superjunction diode is related to some technological parameters, which could be critical to obtain the expected electrical performances, i.e. trenches verticality, P regions implantation along the trenches sidewalls and control of dielectric filling. Indeed, to ensure a perfect charge balance between N and P regions, it is necessary to optimize the fabrication of the deep trenches to obtain etching sidewalls as vertical as possible with a lowest surface roughness. Another critical step is the filling of the deep trenches by a dielectric: breakdown voltage of the termination is dependent on its electric properties i.e. on the values of critical electric field ( $E_{Cd}$ ) and permittivity ( $\epsilon_{rd}$ ). We present the different works we have performed in order to optimize these different technological steps.

##### 4.1. Verticality of the trenches

The Deep Reactive Ion Etching (DRIE) is the more suitable technique to obtain a perfect verticality of trenches sidewalls: it consists on an anisotropic etching based on an alternation of a Si etching step with  $\text{SF}_6$  and a passivation step with  $\text{C}_4\text{F}_8$ . The main etching factors we can act on are the bias power, the pressure, the etching and passivation cycle times.

We have studied the influence of the passivation cycle time on the trench verticality. For an etching time fixed at 2 s, we have varied the passivation time from 1.5 s to 6 s for a gas flow rate fixed at 250 sccm. Between 1.5 s and 3 s, the etching profile is positive (the top width is wider than the bottom one) whereas beyond 3.5 s, the profile is negative. The most vertical profile is obtained for a passivation time of 3.5 s, as shown on **Figure 8** for 5  $\mu\text{m}$  wide and 53  $\mu\text{m}$  deep trenches (etching time of 25 min): the difference between the width at the top and the bottom of the trench is 0.1  $\mu\text{m}$ .



*Figure 8: SEM pictures of a cross section for 25 min DRIE etching and a  $C_4F_8$  passivation time of 3.5 s: the trenches are 5 μm wide and 53 μm deep*

One of the characteristics of High Aspect Ratio (HAR) silicon etch using the Bosch process (Laermer et al., 2003) is the scalloped shape of the sidewalls which is the consequence of the etching and passivation cycles alternation. The peak-to-valley distance can reach a 100 nm range (**Figure 9.a**). One of the critical step for the superjunction diode fabrication being the P implantation on the deep trench sidewall, it is necessary to reduce the scallops size. To do that, after trenches etching, we perform a thermal oxidation: a 260 nm  $SiO_2$  growth allows a 100 nm silicon material consumption. After a buffer HF wet etching, the oxide is eliminated and the peak-to-valley distance is reduced: it is lower than 50 nm as shown in **Figure 9.b**.

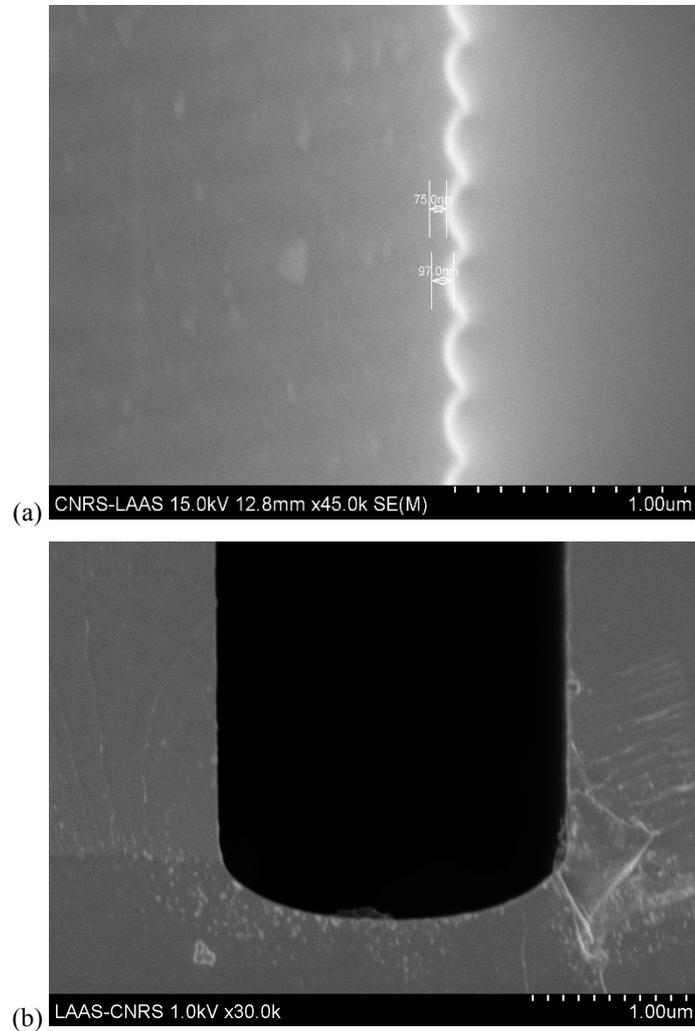


Figure 9: SEM picture of the scalloped shape of the trench sidewall after DRIE (a) after Si oxidation and buffer HF etching for scallops size reduction (b)

#### 4.2. Reduction of the “ARDE” effect

The Aspect Ratio Dependent Etching effect (ARDE) is a limiting factor for the Bosch DRIE process: narrow trenches are etched slowly than large ones due to the reduction of ion bombardment and gas transport at the bottom of narrow and deep features (Chung, 2004). For our structure, the termination trenches are 40  $\mu\text{m}$  wide whereas the trenches of the active central cells are 6  $\mu\text{m}$  wide, inducing a deeper etching for the large ones. For example, for an etching time of 25 min and a 3.5 s

$C_4F_8$  passivation time, the depth obtained for the central cells is  $53 \mu\text{m}$  while it is around  $95 \mu\text{m}$  for the termination trenches. From an electrical point of view, it does not influence the breakdown voltage because the termination over crosses the epitaxial layer, fixed at  $60 \mu\text{m}$  for a  $600 \text{ V}$  structure, and does not affect the balance charge. However if trenches are too deep, their dielectric filling becomes problematic.

In order to minimize the ARDE effect, we developed a technological process for the reduction of the etch rate difference between narrow and large trenches. A thermal silicon oxide mask is added only on top of the largest aperture before the photolithography resist patterning. The role of this oxide is to delay the etch beginning on the largest trenches.

The influence of the oxide thickness on etching depth for various trench widths is reported on Figure 10, for 25 min and 65 min etching times. For the latter, using a  $300 \text{ nm}$  thick oxide, the depth gap between  $6 \mu\text{m}$  and  $40 \mu\text{m}$  features is  $70 \mu\text{m}$ , and the depth gap between  $6 \mu\text{m}$  and  $80 \mu\text{m}$  ones is  $100 \mu\text{m}$ . In the case of a  $1.6 \mu\text{m}$  thick oxide, the depth gap between  $6 \mu\text{m}$  and  $40 \mu\text{m}$  features is  $5 \mu\text{m}$ , and the depth gap between  $6 \mu\text{m}$  and  $80 \mu\text{m}$  ones is  $20 \mu\text{m}$ . These results are illustrated by the SEM pictures reported on Figure 11, for a 65 min DRIE etching time and a 3.5 s passivation time, and for  $300 \text{ nm}$  and  $1.6 \mu\text{m}$  oxides (Figure 11.a and 11.b respectively).

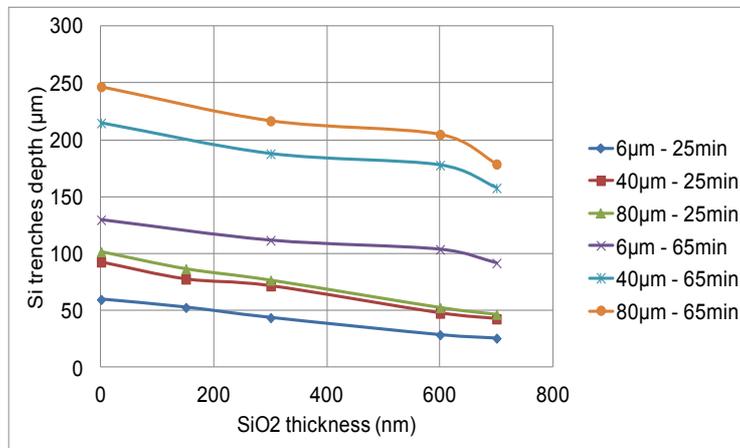


Figure 10: Silicon depth variations versus  $\text{SiO}_2$  mask thickness for 25 min and 65 min etching times and different trench widths ( $6 \mu\text{m}$ ,  $40 \mu\text{m}$ ,  $80 \mu\text{m}$ )

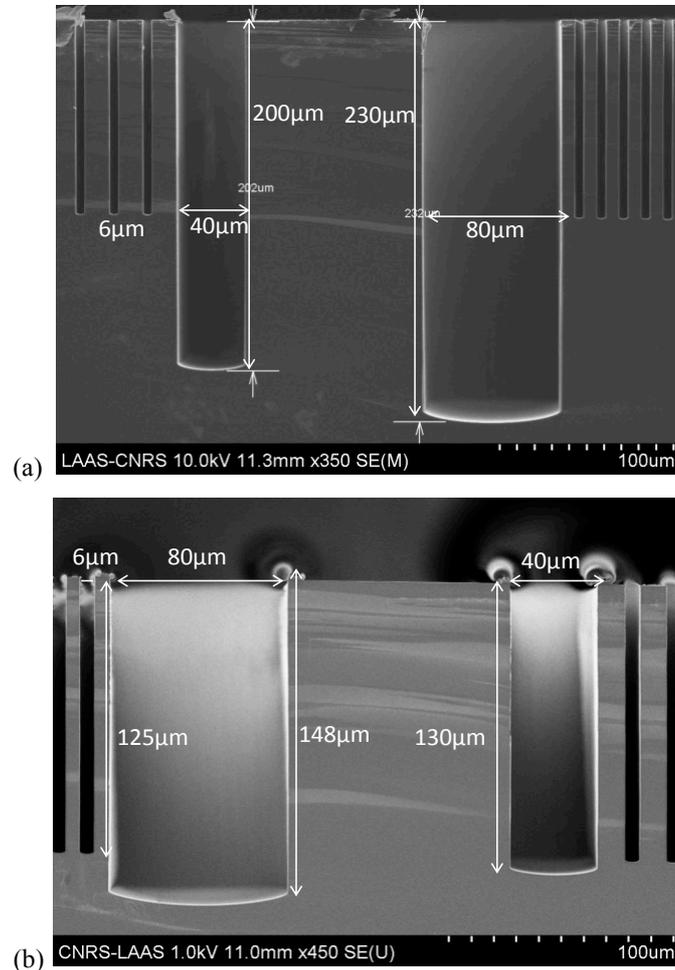


Figure 11: SEM picture of trenches with high aspect ratio ( $HAR > 28$ ) for an etching time of 65min through an oxide layer of 300 nm thick (a) and 1.6  $\mu\text{m}$  thick (b)

#### 4.3. Dielectric filling of the trenches

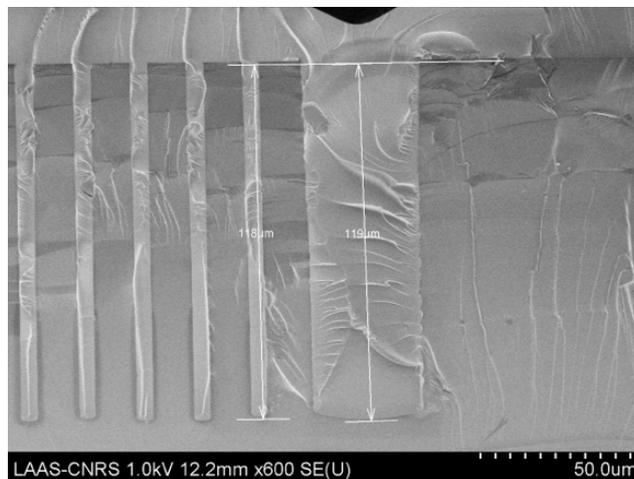
Among the available dielectric materials for trenches filling, the Cyclobutene 4026-46 (BCB) is a good candidate ( $E_{Cd} = 5.3 \text{ MV/cm}$  and  $\epsilon_{rd} = 2.65$ ). Previous works allowed to validate this technological step for 1200 V breakdown voltage diodes (Theolier et al., 2009). However to achieve a complete deep termination trench filling, it was necessary to perform two successive BCB spin-coatings, associated to two chemical-mechanical polishing steps to remove the excess of

dielectric on top of the structure. We have developed a new technological process in order to rend the process more simple with only one deposit of BCB.

We have first worked on the etching step to obtain a same depth for trenches with different widths as shown in paragraph 4.2, thus lowering the necessary BCB quantity. We also optimized the BCB coating parameters: the results are given in Table 2. Due to the high viscosity of BCB material, a small spinner rotation speed (100 rpm) associated to a rest stage favors narrower trenches filling while the spreading step favor the excess material escape. BCB is then soft baked on a hot plate at 90°C for 5 min to remove the solvent and to stabilize the film, followed by hard curing at 250°C for 60 min under N<sub>2</sub> ambient.

*Table 2: BCB spin-coating parameters*

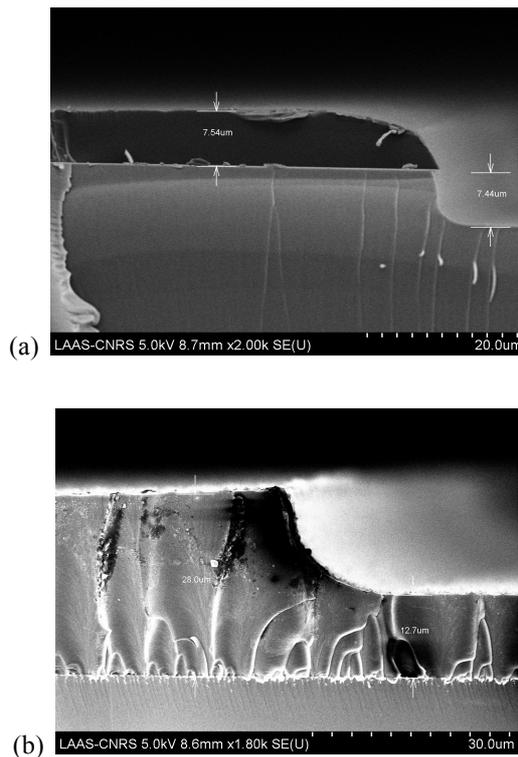
Spin-coating steps	Time	Rotation Speed	Acceleration
BCB dispensing	60 s	100 rpm	100 rpm <sup>2</sup>
BCB spreading	30 s	200 rpm	200 rpm <sup>2</sup>
Rest	10 min		
BCB spreading	10 s	1000 rpm	1000 rpm <sup>2</sup>
Rest	10 min		



*Figure 12 : Cross-sectional SEM view of trenches filled with one BCB spin-coating*

**Figure 12** shows a SEM cross-sectional view of 6  $\mu\text{m}$  and 40  $\mu\text{m}$  wide and 120  $\mu\text{m}$  deep trenches successfully filled with only one BCB spin-coating. Resulting BCB thickness on top of the wafer is 40  $\mu\text{m}$ .

We have investigated the capability to remove the BCB excess by reactive ion etching instead of chemical-mechanical polishing: the challenge is the high thickness to be etched, i.e. tenth of microns. We first studied BCB etching with a photoresist mask using both fluorine and oxygen such as  $\text{SF}_6/\text{O}_2$  gas mixture (Chen et al., 2010): the fluorine removes the silicon in BCB and the oxygen reacts with the carbon and organic content. We analyzed the influence of the plasma etching parameters, i.e. RF power, chamber pressure, gas composition ratio, on the etching rate, BCB selectivity to photoresist and anisotropy. First results are shown in **Figure 13** for a 40  $\mu\text{m}$  BCB layer and 14  $\mu\text{m}$  AZ photoresist: after 10 min etch (**Figure 13.a**), a same 7.5  $\mu\text{m}$  thickness of resist and BCB has been etched; after 20 min etch (**Figure 13.b**) there is no more resist and half of BCB is etched, i.e. 20  $\mu\text{m}$ . This indicates that BCB and photoresist have the same etch rate, around  $0.75 \mu\text{m}\cdot\text{min}^{-1}$ . We obtained residue-free etching for the applied plasma conditions.



*Figure 13 : Cross-sectional SEM view of BCB etch after 10 min (a) and 20 min (b) with 14  $\mu\text{m}$  photoresist mask,  $\text{SF}_6$  (15 sccm)/ $\text{O}_2$  (200 sccm) plasma, 40 W RF power, and 0.2 mT chamber pressure*

However BCB etching is not anisotropic: this is due to the plasma conditions to be optimized but also to the slope observed in the resist profile after the soft-bake step (**Figure 13.a**). The resist profile is transferred into BCB layer during etch. So future works will concern, in particular, the optimization of the etch mask: we will investigate either a thicker resist layer by controlling its soft-bake or a metal hard mask such aluminum thin film.

## 5. Conclusion

New technological ways allowing the realization of deep trench superjunction devices (diodes or MOS transistors) with a deep trench termination are proposed. We developed a technology based on a single N<sup>-</sup> epitaxial layer and the use of BCB filled, wide and deep trenches associated to boron doping on the trench sidewalls. Previous works have demonstrated the feasibility of such junction termination and have led to the fabrication of a 1200 V Deep Trench Termination Diode. We chose to validate our technological choice by fabricating a Deep trench Superjunction Diode (DT-SJDiode) for 600V applications.

By means of Sentaurus TCAD 2D-simulations, we have first determined the optimal physical and geometrical parameters leading to a best ‘Breakdown voltage/on-state resistance’ trade-off. For example, for a N<sup>-</sup> epitaxial region doping concentration of  $3 \times 10^{15} \text{ cm}^{-3}$ , a distance between two central trenches of 8.5  $\mu\text{m}$ , and a trench termination width of 40  $\mu\text{m}$ , the breakdown voltage is 595 V and the specific on-state resistance is 126  $\mu\Omega.\text{cm}^2$ .

We presented technological results focusing on the control of deep trench verticality by Deep Reactive Ion Etching technique, and the trench filling with dielectric. We have studied the influence of SF<sub>6</sub> etch and C<sub>4</sub>F<sub>8</sub> passivation times on resulting trench verticality: the best anisotropy for 6  $\mu\text{m}$  wide central trenches and 40  $\mu\text{m}$  wide termination trenches is obtained for the couple SF<sub>6</sub> (2 s)/ C<sub>4</sub>F<sub>8</sub> (3.5 s). A thermal oxidation after the etch step allows to reduce the size of the scallops that appear on the trenches sidewalls due to the Bosch process.

Finally we have successfully filled deep and wide trenches by optimizing the BCB spin-coating parameters: dispensing rotation speed down to 100 rpm, implementation of two 10 min rest steps improve BCB spreading and its flowing along the trenches. The BCB excess removing by reactive ion etching is under study: first encouraging results give an etch rate of 0.75  $\mu\text{m}.\text{min}^{-1}$  with a SF<sub>6</sub>/O<sub>2</sub> gas mixture.

A complete fabrication process, integrating the above technological steps associated to the boron implantation on the trenches sidewalls, is in progress for the realization of 600 V DT-SJ Diode and DT-SJMOSFET.

## 6. Acknowledgements

*For this work, the authors acknowledge the support of the French RENATECH Network and the French Agence Nationale de la Recherche (ANR) under reference ANR-2011-B509-033 ("SUPERSWITCH" project)*

## 7. References

- Chen Q. (2010). Characterization of reactive ion etching of benzocyclobutene in SF6/O2 plasmas. *Microelectronic Engineering*, 87, p. 1945-1950
- Chung C-K. (2004). Geometrical pattern effect on silicon deep etching by an inductively coupled plasma system. *Journal of Micromechanics and Microengineering*, 14, p. 656-662
- Dow Chemical Company Processing for CYCLOTENE 4000 Series Photo BCB Resins, Février 2005.
- Fujihira T. (1997). Theory of semiconductor superjunctions devices. *Japanese Journal of Applied Physics*, Vol. 36, p. 6254-6262, 1997.
- Learner F. (2003). Method of anisotropic etching of silicon. Patent n°6,531,068 B2.
- Lorenz L. (1999) COOLMOS™ – a new milestone in high voltage power MOSFET. *ISPSD*, p. 3-10.
- Nizou S. (2006). Deep Trench doping by plasma immersion ion implantation in silicon. *16th International conference on Ion Implantation Technology*, p. 229-232.
- Sagio M. (2000). MDMESH™: innovative technology for high voltage power MOSFETs. *ISPSD*, p. 65-68.
- Théolier L. (2008). Conception de transistors MOS haute tension (1200 V) pour l'électronique de puissance. Thesis.
- Théolier L. (2009). A new junction termination technique: the Deep Trench Termination (DT2). *ISPSD*, p. 176-179.
- Théolier L. (2009). A New Junction Termination Using a Deep Trench Filled With BenzoCycloButene. *IEEE Electron Device Letters*, Vol. 30, no. 6, p. 687-689.