Under Voltage Lock-Out Design Rules for Proper Start-Up of Energy Autonomous Systems Powered by Supercapacitors

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Abstract. This paper deals with the issue of the initial start-up of an autonomous and battery-free system powered by an energy harvester associated with a storage subsystem based on supercapacitors initially discharged. A review of different low power Under Voltage Lock-Out (UVLO) solutions used to delay the load start-up and to avoid a useless discharge of supercapacitors is presented and discussed.

1. Introduction

For battery-powered systems, the supply voltage remains quite constant, whatever the state of charge of the batteries (within extreme limits) and start-up of powered systems (load) is not an issue. Conversely, in a battery-free system powered by an energy harvester, a storage unit is required as a buffer stage to adapt for current surge from the load and as a charge reservoir when the energy source is temporarily absent. This storage unit is generally based on a supercapacitor (V_{SC}) whose voltage across it is charge dependent. Considering the classical topology of two supercapacitors in series, the voltage level varies typically between 0 and 5.0 V. On the other hand, the load usually works properly within a limited range [V_{MIN} - V_{MAX}], raising the following issues.

First, generally speaking, the device's consumption is null or negligible for a voltage below V_0 (with $V_0 < V_{MIN}$). When the supply voltage reaches V_0, the device consumption increases to a certain level. If this level is greater or equal to the harvested power, supply voltage will never reach V_{MIN}, a necessary condition for a proper start-up of the system. Therefore, in this situation the storage device and the load must be disconnected until $V_{SC} > V_{MIN}$.

Moreover, a power peak is often required for load start-up inducing a voltage drop across the supercapacitors. As it takes place when the voltage value is close to V_{MIN}, the system is likely to stop immediately. To avoid such a problem, it is necessary to delay the start-up.

Finally, when harvested power vanishes, the system relies on stored energy only. When consequently V_{SC} falls below V_{MIN}, the load stop properly working, but its consumption will remain stable or will even increase. It will then uselessly empty out the supercapacitors, and will delay the next start-up. In such a case, it is of interest to disconnect the load as soon as the decreasing voltage reaches V_{MIN}.

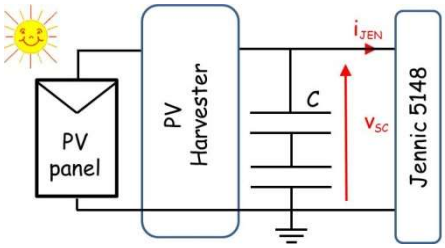

Figure 1. Schematic of the structure considered.

To illustrate the above phenomenon, we built the system described in figure 1. It is made of the following devices:

- energy storage is achieved by two Maxwell PC10 supercapacitors in series,
- the harvested energy is supplied by Solarex MSX-01 photovoltaic panels (V_{OC} = 10V, I_{SC} = 150 mA @STC,)
- an energy management device incorporating a DC/DC buck converter and a microcontroller sits between the above panels and supercapacitors. [**1**].
- the load is an JN5148 Wireless Microcontroller Module targeted at low-power wireless networking applications, programmed for a measurement / transmission each 8 s, and switching to sleep mode in between. The discussed [V_{MIN} - V_{MAX}] supply voltage nominal interval is [2.3V - 3.6V].

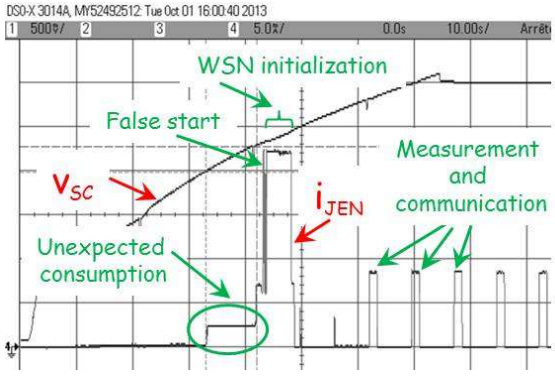

Figure 2. *Cold start* in the case of a high harvested power: voltage across the supercapacitors, V_{SC} and current provided to the load, I_{JEN}.

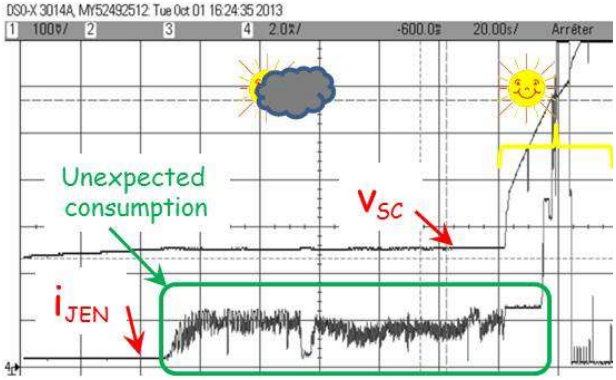

Figure 3. *Cold start* in the case of an initial low harvested power; initial V_{SC} =2.0V

In figure 2, V_{SC} and current I_{JEN} supplied to the Wireless Microcontroller Module are plotted vs. time, when supercapacitors are initially empty and panels are benefiting from a good illumination (~1000 W/m^2). Initially V_{SC} regularly increases and the module draws no current. When V_{SC} reaches 2.0 V, the supplied current establishes itself at 2mA until V_{SC} reaches the lower threshold voltage of the nominal bias voltage interval (i.e 2.3V). During this phase a few false starts corresponding to higher and abnormal current values can be observed. Then, while V_{SC} is still increasing, initialization of the Wireless Microcontroller Module takes place, requiring a high current. Later on, current peaks correspond to measurement and data transmission. It appears that a lot of energy is required during system start-up. If this energy cannot be supplied (reduced illumination), start-up is not possible (see figure 3), and because of the current drawn by successive attempts, this energy will never be stored in the supercapacitors.

The purpose of an Under Voltage Lock-Out (UVLO) strategy is to deal with this problem.

2. UVLO solutions

A UVLO system is made of two devices:

- a blocking device (switch) controlling the load biasing,
- a control logic. [**2**]

Below we present various implementations of these two functions.

2.1. Blocking system

2.1.1. Simple switch located on the ground rail.

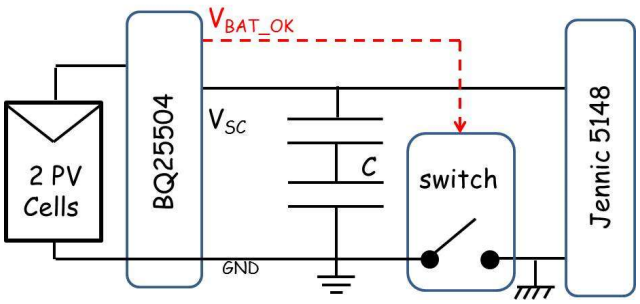

Figure 4. *Structure with the switch on the ground line.*

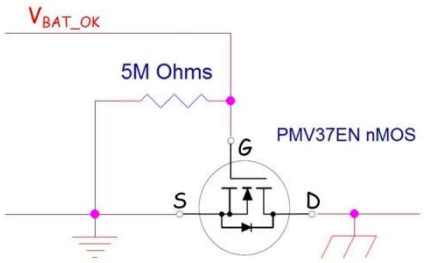

Figure 5. *Switch on the ground line.*

This is a straightforward implementation (see figures 4 and 5) using an NMOS transistor as a switch whose control voltage V_{GS} comes from the control logic. An NMOS is chosen because its body diode will never be forward biased. The 5 M□ resistor connected to the gate guarantees an OFF state when V_{BAT} is low during a *cold start*; its high value limits the current between control signal V_{BAT} and ground when V_{BAT} is high.

The following characteristics are required for the NMOS transistor,

- a gate threshold voltage compatible with the control logic output,
- a R_{DSON} value as low as possible to limit energy losses and voltage drop between supercapacitors and wireless module,
- a nominal current compatible with the maximum current drawn by the load.

The main drawback associated with this topology is the introduction of two ground references, likely to complicate measurement in a prototyping phase. An alternative is presented below.

2.1.2. Switch located on the supply rail.

Figures 6 and 7 present this alternative where the switch is inserted in the supply rail, keeping a single ground reference. Details about the control logic are given in figure 8.

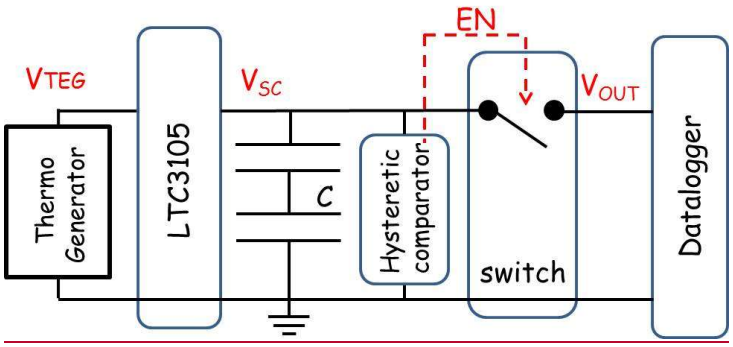

Figure 6. *Structure with the switch located on the supply rail.*

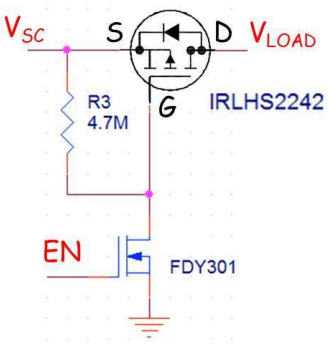

Figure 7. *Switch on the supply rail.*

The switch here is a PMOS transistor which gate is controlled by an NMOS. The intrinsic diode of the MOS asks here for a PMOS to get an initial OFF state during system start-up. When *high*, the logic output turns ON the PMOS by pulling its gate to ground through the NMOS, and conversely turns it OFF when *low* by turning OFF the NMOS, allowing the PMOS gate to be pulled up to V_{SC} through the pull up resistor.
Most important parameters to consider are:

- a low R_{DSON} of the PMOS, for reasons already discussed in the previous paragraph,
- an NMOS threshold voltage compatible with the control logic output,
- a low *slew rate* of the PMOS switch to limit the *inrush* current [**3**].

Such a structure can easily be implemented using discrete devices, or by choosing a dedicated integrated circuit as explained below.

2.1.3. Load switch
An integrated load switch contains a P-channel MOSFET that operates over an input voltage range (for example, 1.0 V to 3.6 V for a TPS22901). The switch is controlled by an on/off input, which is capable of interfacing directly with low-voltage control signals. Optionally, an on-chip load resistor is added to avoid a floating rail and for output quick discharge when the switch is turned off.
An integrated load switch offers:

- a low R_{DSON},
- a low threshold control inputs,
- an ultra-small packaging,
- a quiescent and shutdown current below 1µA,
- an internally controlled slew rate

Nevertheless an even simpler solution is possible as detailed below.

2.1.4. Pin "Enable" or execution of a priority interrupt
When the load to be powered exhibits an *Enable*-type input command, the simplest implementation of an UVLO procedure lies in the use of this command [**4**], provided first that the command logic outputs are compatible, and then that the corresponding quiescent current is low enough. If the load is a microcontroller, an input command triggering a priority interrupt execution deactivating peripherals and switching to a deep sleep mode is also an option (as an example, we measure 2µA in deep sleep with the Jennic 5148).

3. Control logic

With respect to the control logic, it has to monitor V_{SC} and to determine the logic command to be applied to the switch or circuit inputs. A simple practical solution is a hysteresis comparator using two thresholds V_{IH} and V_{IL}, with $V_{IH} = V_{MIN} + \Delta V$ and $V_{IL} = V_{MIN}$.[**5**]
ΔV is a voltage (and therefore an energy) margin allowing extra power consumption during start-up preventing V_{SC} from falling rapidly below V_{MIN} before the end of the transient associated with the start-up itself. Worth to be mentioned is the voltage drop associated with the series parasitic resistors of the supercapacitors, adding an extra component to V_{SC} drop for high currents.

3.1. Hysteresis comparator with discrete elements
The driving circuit on figure 8 is realized with discrete elements using an ultralow power comparator. It includes a voltage reference and is supplied by the supercapacitor voltage.

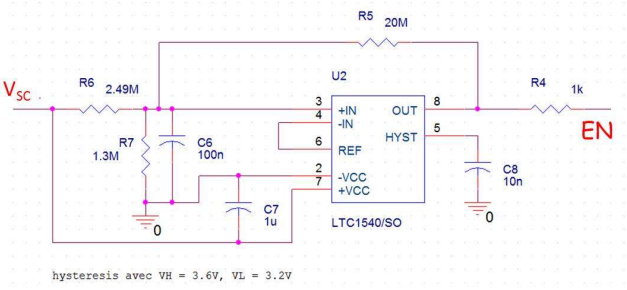

Figure 8. *Comparator with hysteresis.*

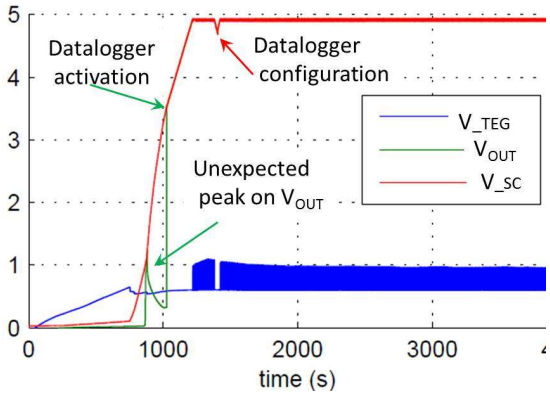

Figure 9. *Start-up sequence.*

Passive component values are chosen to minimize energy losses. Total consumption of the circuit of figure 8 is about 2µA. It has been implemented for the topology depicted in figures 6 and 7. In this case the power source is a thermoelectric generator connected to a DC/DC converter, whereas the load is a commercial datalogger. Corresponding experimental results are presented in figure 9. It can be seen that, even though the datalogger is actually turned on as soon as V_{SC} reaches the high trip voltage V_H=3.6V, an unexpected voltage peak takes place on the UVLO output when V_{SC} = 1V. Such a parasitic behavior is caused by the hysteresis comparator, which is transiently unable to maintain its output low as its supply voltage is increasing, yet below its minimum value (2V). This can be avoided by selecting an NMOS with a threshold voltage greater than the comparator's minimum supply voltage. Fortunately, in this configuration the peak is too small to turn on the datalogger, and disappears as soon as the comparator is properly supplied.

3.2. Integrated hysteresis comparator

The desired feature is often included on commercial energy harvesting components. As an illustration, Texas Instruments BQ25504, which is a boost charger IC for ultra-low power energy harvesting, a V_{BAT_OK} output command is available, and three external resistors can adjust thresholds V_{IH} and V_{IL}. If energy source disappear, this energy harvesting device stays active and takes its supply power from the supercapacitors and drains 90 µA. This value should be compared with the 2 µA consumption only of the hysteresis comparator on Fig. 8.

4. Conclusion

We have presented the reasons and main implementations of an Under Voltage Lock-Out (UVLO) strategy when intermediate storage in supercapacitors is used. Solutions using integrated circuits are the more attractive in terms of simplicity and cost. Discrete implementations are the more appropriate while in a design and prototyping phase and can be used as a reference vs. power consumption.

5. References

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