# Compact Phase Shifting Cell Based on Micro-Strip Slow Wave Lines

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***Abstract* — This paper addresses the design, the simulations and the measurements results of an original and compact MMIC phase shifter using micro-strip slow wave lines implemented in a 0.25µm SiGe BiCMOS process for Ku-band applications. The simulations and the experimental results demonstrate interesting performances compared to classical phase shifter topologies.**

## I. Introduction

Phase shifters are key components in phase array systems where they achieve beamforming functions. The modern phase array systems developed for telecommunications applications need an increased flexibility and real-time electronic command and control functions. A typical core-chip used for beamforming applications requires a large number of RF phase control points. The performance of such core-chip circuits drives the performance of the final beamforming systems [1]. As example, the classical solution adopted for the beamforming system of the broadcasting satellites involves a 'hybrid' approach. The digital circuits used for command and control functions in the beamforming system are implemented in CMOS based technology while the analog RF functions (phase-shifting and attenuator cells) are mainly implemented in GaAs technology. This 'hybrid' approach increases the complexity, the size and the cost of the beamforming system.

The integration capability on a silicon chip is a key issue allowing a significant footprint reduction beside the low power consumption [2]-[3]. Consequently, due to the characteristics of Si technologies, a large number of low cost phase shifters have been investigated [4]-[5].

In this paper, we introduce a novel and original BiCMOS phase shifting cell/topology based on the use of micro-strip **S**low **W**ave **L**ines (SWL). This topology leads to a compact footprint (compared with the footprint of 'classical' topologies [3]-[5]) while a phase shift below 22.5° is targeted. Also, this topology constitutes a new alternative to other SWL phase shifters [6].

The section II focuses on the proposed topology of the SWL **P**hase **S**hifter (SWL PS). The simulated and experimental results obtained for the manufactured 11.25° SWL PS cell are presented in Section III. The performances of the SWL PS cell can be further improved by using body floating or substrate connection techniques as discussed in Section IV.

## II. Phase Shifter Design

This phase shifter uses SiGe cold FETs (no bias current) as switches. The phase shift is obtained as a delay between the two signal paths (Fig.1 a). The first transmission line is a classical **M**icro-**S**trip **L**ine (MSL) and the other transmission is a **S**hielded **M**icro-**S**trip **L**ine (S-MSL). For comparison purposes, the 'classical' topology is represented in Fig 1 b. This topology is valid for phase shifter between 90° and 11.25° [4][5].

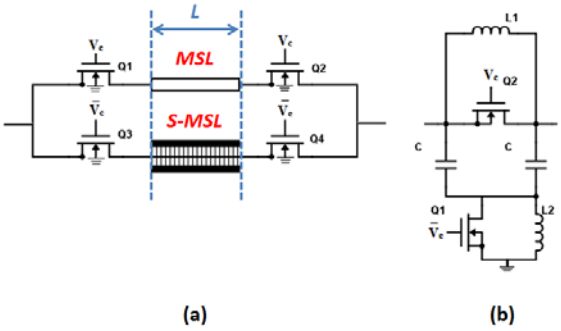


Fig. 1. Proposed phase shifting cell based on SWL
(a) proposed topology
(b) example of the classical topology

The SWL used to obtain the targeted phase shift is a two layer S-MSL [7] that allows a more compact structure compared to the classical Shielded Coplanar Waveguide (S-CPW). The stack layer of the process is presented in Fig. 2. It offers two thick layers (TM2 and TM1) fitted for carrying the signal and three thin layers (M3, M2 and M1).

As depicted in Fig. 3, the conducting strip is located on the top metal layer (TM2) while the metal strips composing the ground plane are located on the two layers (TM1 and M3). This disposition of the ground strips on two metal layers prevents the E-field from penetrating the silicon and improves the Q factor [8].

The slow wave line path has been implemented in 0.25µm SiGe BiCMOS process and measured by using a VNA (Anritsu ME7808A).

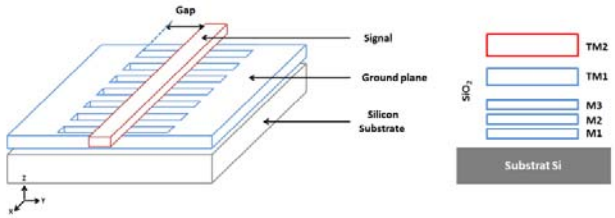


Fig. 2. S-MSL topology and cross section of the BiCMOS process

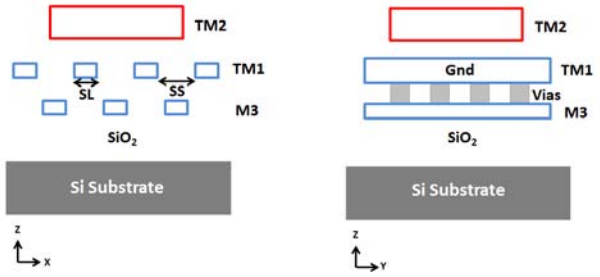


Fig. 3. Cross-section view of the SWL structure

The S-MSL was obtained after the optimization of the Strip Length (SL), the Strip Spacing (SS) and the Gap parameters. The experimental results show an improvement of the phase constant by a factor 2.4 compared to a classical MSL (at 15GHz) while the attenuation constant remains almost equivalent [7].

## III. Results

The phase shifting cell was fabricated using IHP 0.25µm BiCMOS process. The S-Parameters measurements were performed with a VNA using a standard SOLT calibration procedure. A photo of the dye can be seen on Fig. 4. The size of the phase shifter excluding the pads is 300µm x400µm. In order to simulate the behaviour of the cell, SWLs were electromagnetically simulated on HFSS and then imported on ADS to be combined with the simulation of the transistors. The targeted phase shift was 11.25° (with an authorized deviation of +/- 3°) in the Ku-band: 10.7 GHz -14.5 GHz. The experimental results for ON ($V_c$=2.5 V) and OFF ($V_c$=0 V) states are shows in Fig. 5 (insertion loss) and Fig.6 (return loss). The measurements show important insertion loss for the phase shifting cell. This drawback can be explained by the fact that the bulk of every transistor is directly connected to the ground. Solutions to correct this issue are proposed in section IV. The return losses are under -8.5dB for the targeted band (10GHz - 15GHz). The difference between the simulations and the measurements can be explained by (i) the impact of the pads (aluminium) that is not taken into account in simulations and (ii) the insertion losses of the transmission lines (especially S-MSL) that are underestimated in HFSS.

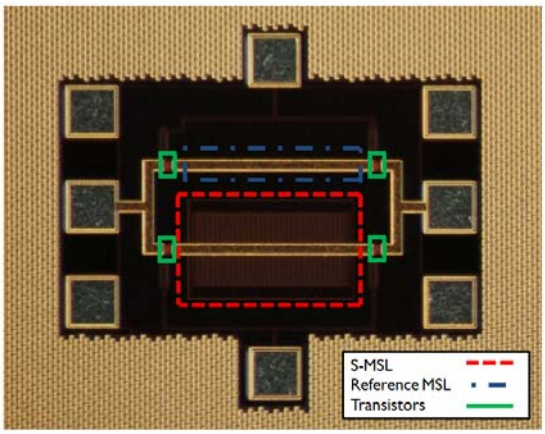


Fig. 4. Photo of the phase shifting cell (250µm x 400µm excluding pads)

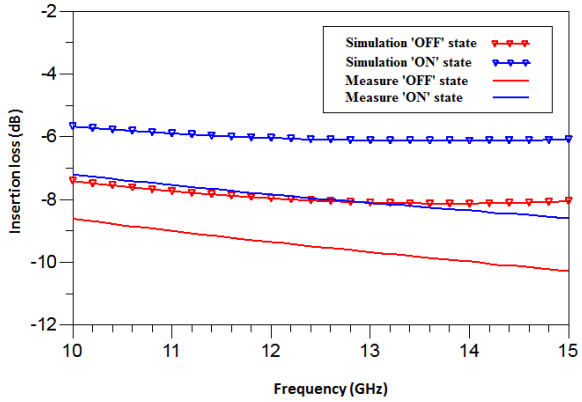


Fig. 5. Insertion loss of the SWL PS for ON/OFF states

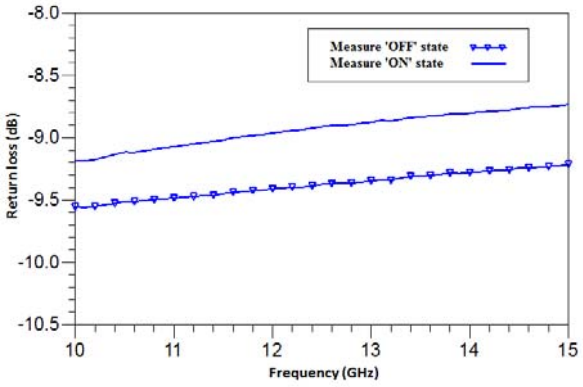


Fig. 6. Return loss of the SWL for the ON/OFF states

Fig. 7 shows the simulated and measured phase shift of the SWL PS as function of frequency. The differences between the simulations and the measurement are due to the overestimated (in the simulation) phase advance of the SWL line. The FETs being used as switches do not consume DC current (the measured DC current is less than 0.1 µA). Moreover the SWL PS exhibits a quite small linear variation of the phase shift in the targeted frequency band that is very useful from an application point of view.

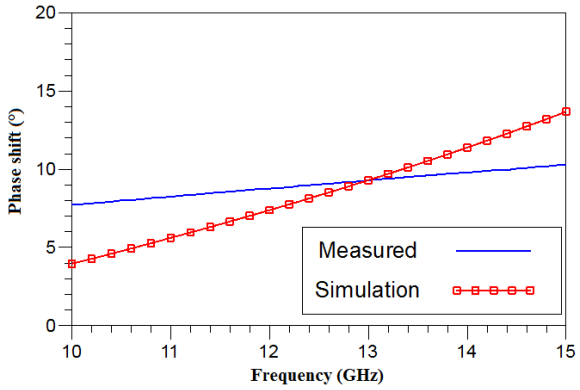


Fig. 7. Phase shift of the SWL PS.

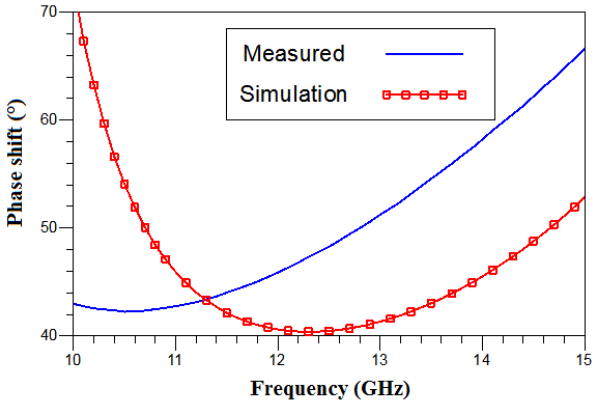


Fig 8. Phase shift of the 'classical' 45° PS cell

This cell is even more promising when compared to a 'classical' MMIC phase shifter [2]-[4]. A 11.25° hybrid/classical phase shifter was fabricated on the same run for comparison purposes. Unfortunately this circuit was impacted by a (not detected during design rule check) layout error and the experimental results are not exploitable. However a 45° classical phase shifter cell was fabricated on the same run. The inductors and capacitors values were calculated by the equations given in [4] ($L_s$=450pH, $L_p$=1050pH, C=105fF). This cell allows us to check the correlation between the adopted simulation technique under Cadence/ADS and the experimental results. Fig. 8 shows the simulated and the experimental results for the 45° classical PS cell.

Fig.9 demonstrates that the SWL-PS topology is more compact as compared with the classical PS topology. The footprint of the SWL-PS is reduced by a factor 3.5 as compared with the footprint of the 'classical' phase shifter when a phase shift of 11.25° is targeted.

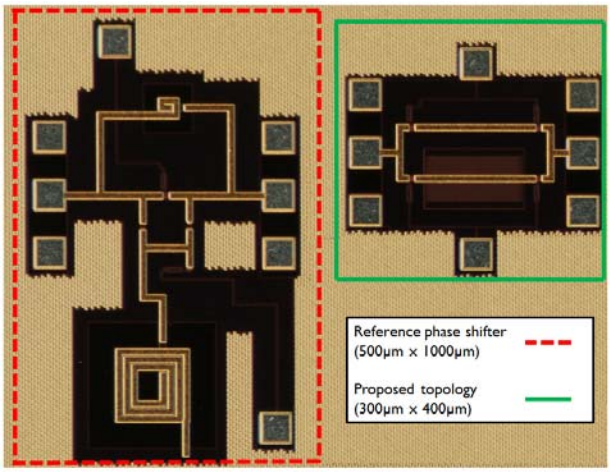


Fig 9. Size comparison between hybrid topology and SWL based solution

## IV. Discussion

As presented in section III, the insertion losses of the phase shifting cell are quite important. Retro-simulations were performed in order to isolate the source of the losses and two solutions are proposed to correct this drawback. It was been found that the main part of the losses was generated by the transistors. The losses added by the switching FETs can be reduced by [8]: (i) connecting the bulk of the FETs to their source (**B**ulk **C**onnected to **S**ource: BCS) and (ii) using the **B**ody **F**loating (BF) technique. BF technique consists of the connecting a 5kΩ resistor to the bulk of the transistors [8]. BF technique improves also the linearity and the return loss of the cell. The impact of these techniques (BF and BCS) was simulated by using a co-simulation approach. HFSS software was used for the electromagnetic simulation of the S-MSL. The obtained S-parameters (by HFSS simulation) were injected in ADS software that was used for circuit simulation.

Fig. 10 (insertion losses) and Fig. 11 (return losses) show the experimental and simulated results for the manufactured SWL-PS compared with the simulated results obtained by using the proposed BCS and BF techniques. As depicted in Fig. 10 and Fig. 11 the use of BF or BCR techniques allows the reduction of the insertion loss and the improvement of the return loss. The BF technique improves also the linearity of the PS cells as represented in Table I (simulation results). The 1dB input compression point is improved with at least 6 dB as function of the topology and of the state (ON/OFF) of the PS.

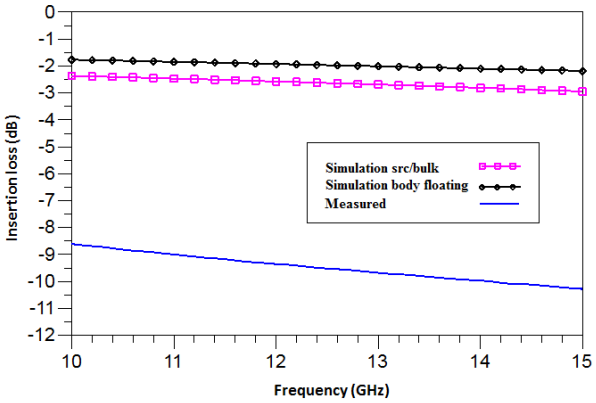


Fig 10. Insertion loss (simulation) of the SWL PS by using BF (diamond marker) and BRC (square marker) techniques compared with the measured results of the fabricated SWL PS (no marker).

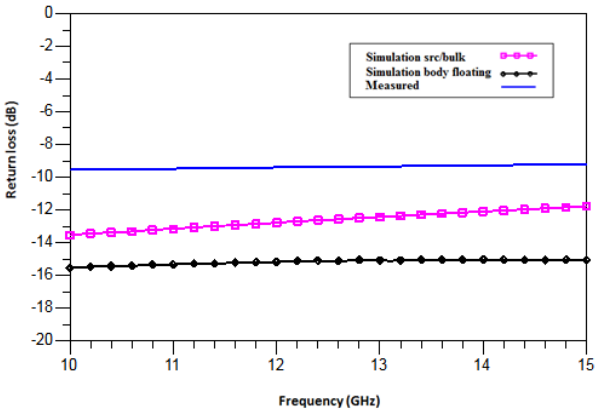


Fig 11. Return loss (simulation) of the SWL PS by using BF (diamond marker) and BRC (square marker) techniques compared with the measured results of the fabricated SWL PS (no marker).

| | P1dB (dBm) | |
|---|---|---|
| | *P1dB (dBm):OFF state* | *ON state* |
| PS 45° | 3.65 | 17.9 |
| PS 45° + BF | 11.55 | 24.55 |
| PS 11.25° | 3 | 12 |
| PS 11.25° + BF | 11 | 22 |
| SWL PS | 15 | 19 |
| SWL PS +BF | 23 | 29.2 |

TABLE I.
1dB COMPRESSION POINT OF THE PHASE SHIFTER CELLS

A new run including an optimized version of the 11.25° SWL-PS cell with pads allowing the access to the bulk is currently in fabrication and more experimental results will be available for the Conference.

## VI. Conclusion

This paper presents an original and compact phase shifter topology using micro-strip slow wave lines (SWL-PS). The proposed phase shifter exhibits a very low DC power consumption and is a more compact solution compared to the classical hybrid topologies: the footprint is reduced by a factor 3 for a phase shift of 11.25°. This solution remains more compact that the classical topology for a phase shift below 22.5° and constitutes a new alternative to the classical phase shifters. The experimental results for the first manufactured sample based on this innovative SWL-PS show good results in terms of phase shift and return loss. The insertion loss is quite important but as demonstrated by the simulation results these insertion losses can be drastically reduced by using BF or BCS techniques. It was also proven that the BF technique improve the input 1dB compression point with at least 8 dB for the SWL PS. Moreover the experimental results demonstrate that the SWL PS topology exhibits a small linear variation of the phase shift over a large frequency bandwidth. This characteristic can be very attractive from critical application (e.g. broadcasting satellite telecommunications) where large uplink and downlink bands should be covered by the same beamforming system.

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