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Gate Defects Analysis in AlGaN/GaN Devices by Mean of Accurate Extraction of the Schottky Barrier Height, Electrical Modeling, T-CAD Simulations and TEM imaging

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Abstract

This paper proposes an investigation focused on the Schottky Diode related electrical behaviors on GaN high frequency technologies. As the Schottky Diode represents the electrical input terminal (the command) of High Electron Mobility Transistors (HEMTs), this study also correlates with some first order degradation in the active channel (current I_{DS}). Non-invasive methods and related models have been used to determine the accurate Schottky Barrier Height (SBH) of the diode in terms of mean value and dispersion; this approach is convenient to evidence different failure mechanisms on virgin and stressed devices that can be correlated with DC or transient electrical parameters. It is shown that according to given temperature windows and I_{GS} ranges, linear relationships can be extracted between the mean SBH and the inhomogeneities of the SBH that appear in forward-biased diode mode. This original approach permits to determine an increase or a decrease of the global SBH after a stress period. Electrical behaviors issued from the proposed non-destructive technique and from electrical modelling of the diode at different temperatures are found to be consistent with Transmission Electron Microscope (TEM) investigations. T-CAD models have also been used and tuned to account for the impact of interface fixed charge density changes on the electrical signatures of the HEMTs.

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1. Introduction

ALGAN/GAN HEMTS are already known for their outstanding performances in microwave field of applications. The high breakdown voltage, electron saturation velocity, cutoff frequency and figures of merit, reveal them as attractive competitors towards the classical solid state transistors developed on silicon and GaAs materials. Using GaN for electronic circuits results in a loss in weight for the system (reduction in the electronic circuit area, power supply and heater or cooling system sizes), with enhanced power capabilities. Yet, limitations like the increase of the junction temperature still represent a challenge to broaden the application fields and markets. Systems working at elevated junction temperature can open the way for new high power and high frequency applications, as for example large volume production dedicated to base stations and other high volume markets, but also to defense and space purposes working under harsh environment. However, reliability investigations are still largely under concern because of the complex electro-thermo-mechanical mechanisms induced in transistors; these reliability studies can only be carried out by using several cross-experiments, or by using destructive techniques in order to evidence the presence of defects. Nevertheless, destructive techniques do not allow concluding about the real impact of the revealed defect on the electrical behavior of the device. The development of new non-invasive (and then non-destructive) experimental approaches can thus bring information about the evolution of electrical signatures before (during) and after application of a stress. This study specifically focuses on gate barrier height related defects, as it impacts the control of the charges in the channel where the electron carriers flow, and interface states causing various reliability issues. Devices were tested under High Temperature Operating Life stress conditions (HTOL). T-CAD model is also developed to account for the fine technological mechanism analysis of the gate control zone, as well as interface fixed charge densities effects on static electrical parameters.

This document is structured as follows: the second section briefly describes the technology under test and the stress conditions used on a sample of 10 devices. The third section is dedicated to the extraction method of the Schottky Barrier Height (SBH) and associated electrical models as well as T-CAD simulations. The last section deals with TEM pictures at the gate edges and under the gate. Lastly, a conclusion is drawn which states the usefulness of the proposed method in terms of technological feedback.

2. Technology under test and under stress

Results on an intermediate step of the final technological declination (under development phase) are reported, with the aim to assess the potential of our method. A batch of ten AlGaN/GaN HEMT devices featuring eight gate fingers, with a width of 125 µm each (technology 0.25 µm gate length), grown on SiC substrate have been used for the study. Two virgin devices are available to evaluate the impact of the HTOL stress operated by UMS at V_{DS}=30V and I_{DS}=100mA/mm, at 175°C ambient temperature (320°C peak junction temperature extracted from simulation model). The measurements reveal a drop on I_{DS} of

about 45% (at V_{GS} = 1 V and V_{DS} = 8 V), an increase of 130% on R_{ON}, and about one decade variation on I_{GS} after 105 hours of HTOL stress. Threshold voltage relative evolutions during the stress are reported in Fig. 1, with final shifts between 5% and 15% on stressed devices (no variation on the two virgin devices also measured – black and red plots).

The demand of having a clean gate contact in power devices is still a key challenge in achieving reliable processes, since some of the failure mechanisms are related to the specific development of the Schottky gate contact. Moreover, the gate terminal (i.e., the command) is the critical zone impacting the performances of the device: shift of the threshold voltage V_{th}, leads to variation of the transconductance gain and of the carriers' density in the two-dimensional electron gas, which become detrimental to the circuit operation and to the system performances.

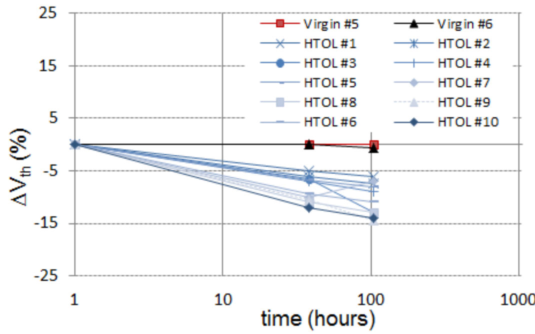


Fig. 1. Impact of the HTOL stress on threshold voltage shift (expressed in percentage).

3. Electrical measurements and modelling of the Gate Schottky Diode

From previous studies [1]–[3], different methods have been developed to investigate the gate contact. Since we are talking about diodes and non-destructive techniques, the most common approach consists in the analysis of the SBH. This part of the work is based on prior studies [4][5], which present an accurate tool for extracting the SBH alone, through the quantification of the defects impact on the global SBH. The technique from [5] brings information about a mean SBH $\overline{\Phi_{Bx}}$ and its relative dispersion σ_{Sx} (inhomogeneity of the barrier, Fig. 2). This technique is non-invasive as it is based on electro-thermal characterization of the device, in open drain configuration (no dissipated power in the

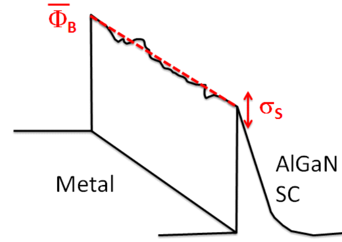


Fig. 2. Representation of the parameters from Werner's method applied to Richardson's model as expressed in [5]: a constant mean value of the SBH ($\overline{\Phi_{Bx}}$) and an associated standard deviation ($\pm\sigma_{Sx}$), i.e. a mathematical expression for the SBH's inhomogeneity.

2DEG). Fig. 3 plots the gate current versus the gate voltage for a virgin device $V_{\#6}$ (Fig. 3.a) and for a stressed device $S_{\#2}$ (Fig. 3.b) at different temperatures. Fig. 4 gives the thermal evolution of the SBH expressed according to its classical electrical expression. Two thermal trends from part of a thermal inflexion point are observed.

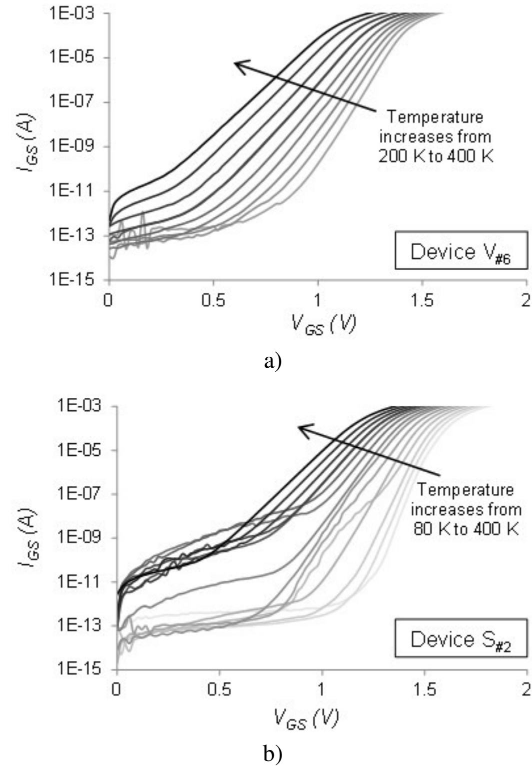


Fig. 3. I_{GS}-V_{GS} measurements versus temperature, with a 25 K step for: a) $V_{\#6}$ (virgin sample) and b) $S_{\#2}$ (stressed sample). Light grey is represented as the lowest temperature, towards dark black as the highest temperature.

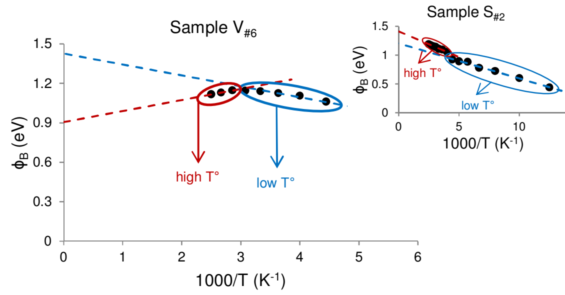


Fig. 4. SBH extracted from classical expression versus temperature for a virgin device $V_{\#6}$ and for a stressed device $S_{\#2}$. An inflexion point separates two temperature zones, next called high T° (red) and low T° (blue).

3.1. Extraction of the mean SBH and dispersion – extracting the accurate ideal SBH

From [5], the determination of the mean SBH and a related dispersion $(\overline{\Phi_{Bx}}, \sigma_{Sx})$ is found not to be sufficient to get the Schottky Barrier Height determined accurately. By varying the I_{GS} current range (considering a 2-decades window) or by changing the temperature, it is demonstrated that:

-the mean SBH evolves largely out of the uncertainty zone of the method, and depends on the I_{GS} range,

-the trend of the mean SBH also depends on the temperature window (next called High Temperature and Low Temperature zones) as depicted in Fig. 4.

Concerning the extraction's accuracy of the mean SBH associated to the method proposed in [5], it has been established that:

-errors due to signal analyzer measurements can be considered insignificant

-an error of less than 7% on $\overline{\Phi_{Bx}}$ is obtained for 50% variation on prerequisite initial conditions on Richardson constant A* and effective mass m*.

-the larger variation is noticed when considering the standard deviation associated to the extracted SBH $\overline{\Phi_{Bx}}$ for each '*x*' sliding window of ΔI_{GS} (Fig. 5). From a dedicated study, it has been established that two decades window for ΔI_{GS} features the lowest variations.

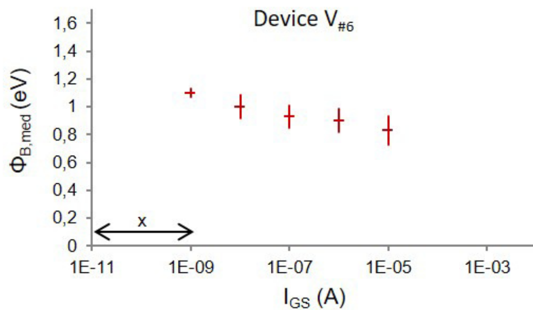


Fig. 5. Example for the extracted mean $\overline{\Phi_{Bx}}$ against the '*x*' sliding window (2 decades ΔI_{GS}), considering the variation of the standard deviation σ_{Sx}, vertical error bars (illustration on virgin device #6).

An original reinterpretation of the pairs $(\overline{\Phi_{Bx}}, \sigma_{Sx})$ has been proposed in [5] by plotting $\overline{\Phi_{Bx}}$ versus σ_{Sx} for all the '*x*' sliding windows of two decades of ΔI_{GS} (Fig. 6 a and b). Therefore, the variation of the mean SBH versus the standard deviation (inhomogeneity) represents the sensitivity of the ideal SBH's value to the defects of the barrier height (inhomogeneity at the metal-semiconductor interface). Thus, the *x*-axis extrapolation at $\sigma_S = 0$ eV represents the ideal Schottky diode without considering any defect ($\Phi_{B\text{-}\sigma_S=0}$; expected theoretical homogeneous SBH).

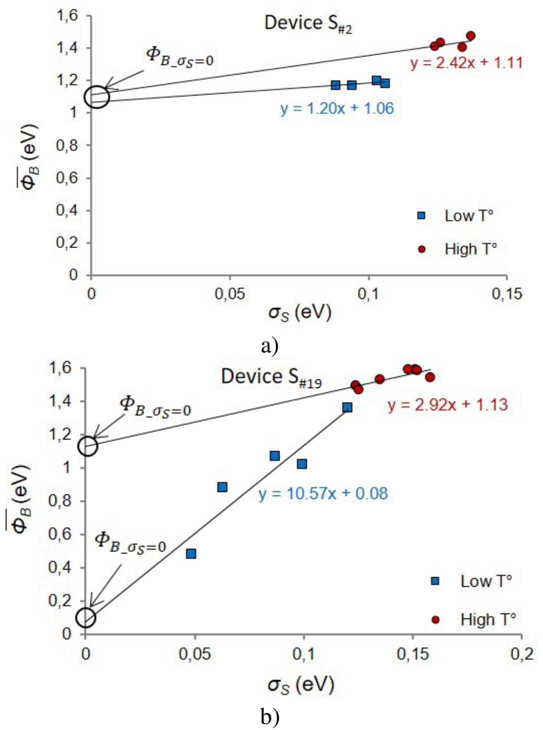


Fig. 6. Variations of $\overline{\Phi_{Bx}}$ versus σ_{Sx} under different gate current ranges (x-sliding gate current window), for: a) $S_{\#2}$ (stressed device #2), and b) $S_{\#19}$ (stressed sample #19). Squares represent the pairs $(\overline{\Phi_{Bx}}, \sigma_{Sx})$ in the low temperature range and circles are the pairs $(\overline{\Phi_{Bx}}, \sigma_{Sx})$ in the high temperature range.

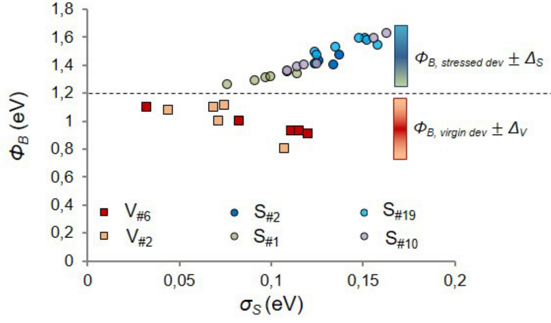


Fig. 7. Variations of $\overline{\Phi_{Bx}}$ versus σ_{Sx} at high temperature, under different gate current ranges (x-sliding gate current window), for 6 devices: (2 virgin samples V# squares – 4 stressed samples S# circles)

The different trends revealed at low or high temperature in Fig. 6.a and Fig. 6.b are consistent with first order and second order defects of the Schottky diode: however, whatever the increasing (stressed devices) or decreasing (virgin devices) impact of the defect within the high temperature window (see Fig. 7), a unique $\Phi_{B\text{-}\sigma s=0}$ is extracted at 1.1eV (±0.1eV). For the lower temperature range, some devices still exhibit an extrapolation of $\Phi_{B\text{-}\sigma s=0}$ at 1.1eV while two devices give an extrapolation at 0eV (see Fig. 6.b, blue squares). This behavior correlates with Energy Dispersive X-Ray spectrometry (EDX) measurements, evidencing a gold conduction path at the edge of the gate as previously shown in [6].

3.2. Electrical models of the gate diode versus temperature

Electrical model has been developed and tuned for all temperatures under study and for all devices under

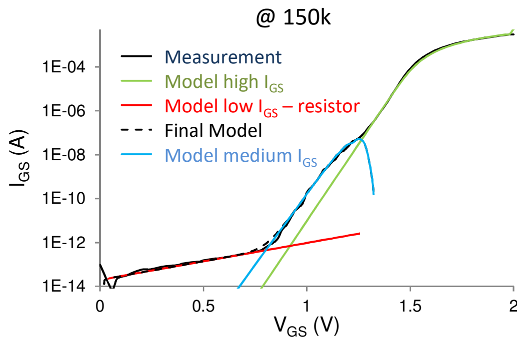


Fig. 8. Example of a model for the gate Schottky diode for a temperature of 150K, featuring different contributions to I_{GS} at low, medium or high I_{GS} levels.

test, revealing different zones in forward biasing conditions that correlate the results from the previous section (TE mode). Fig. 8 reports I_{GS}-V_{GS} plot at 150K where a second diode is identified at medium I_{GS}, but with higher serial resistor (revealing a conduction path not flowing into the quantum well). A highly resistive behaviour is also revealed (ranging from 10^8 to 10^{12} Ω) at low I_{GS} attributed to leakage current at the interface between the SiN passivation and the AlGaN layer (no Schottky diode is involved in this electrical path). This resistive behaviour is reported for 5 devices under test in Fig. 9 (4 devices featuring 4.10^9Ω as illustrated in the inset, and 1 virgin device featuring a higher 10^{12}Ω resistance). The measurements are reproducible.

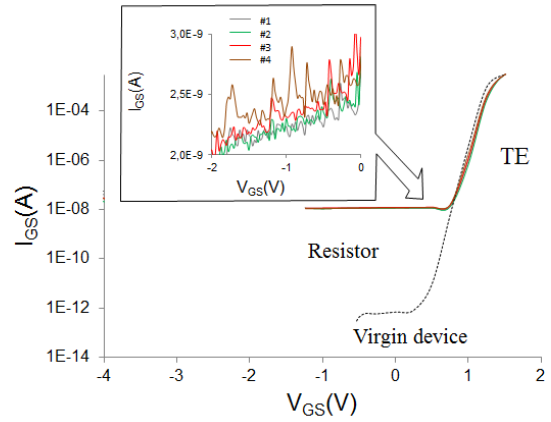
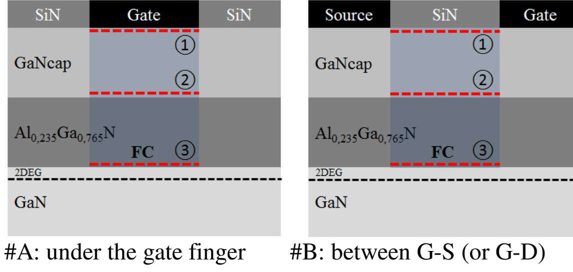


Fig. 9. Extraction of the resistive parasitic behavior from I_{GS}-V_{GS} plots in diode mode (V_{DS}=0V) over a batch of 5 samples (4 devices featuring a 4.10^9 Ω resistance, 1 virgin device feat. 10^{12} Ω resistance), with Thermionic Emission (TE) mode used for SBH extraction.

3.3. T-CAD models

T-CAD simulator (Sentaurus) has been instructed and tuned to match both the stressed and virgin devices on output characteristics I_{DS}-V_{DS} and transfer characteristics I_{DS}-V_{GS} (G_m-V_{GS}). The implementation of the modified structure for the stressed devices is realized considering DC (and transient) electrical measurements performed on I_{GS} and I_{DS}. The principal focus of this section concerns the impact of fixed charges (FC) at the different interfaces from the surface to the active 2DEG, under the gate and between gate-source and gate-drain zones as depicted in Fig. 10.

The different zones where the fixed charges are considered are the gated zone (#A under the gate finger) and the ungated zones (#B between gate and source, or gate and drain). Then, simulations are



#A: under the gate finger #B: between G-S (or G-D)

Fig. 10. HEMT cut view pattern for Fixed Charges (FC) density impact evaluation on electrical behaviors before and after stress application.

performed at three different interfaces: ① FC under the gate metal (#A) or passivation layer (#B), ② at the GaNcap/AlGaN interface and ③ at the AlGaN/GaN (2DEG) interface. These FC locations at ①, ② and ③ are considered independently and simultaneously. Only the FC density at the AlGaN/GaN interface ③ is found to be critical to the variations of I_{DSS}, R_{ON} and V_{th} (weak contribution of FC located at ② and no impact of FC at ①). Fig. 11 reports on the intrinsic transconductance gain g_m variation for different FC densities as depicted in #A, under the gate finger. Only the threshold voltage V_{th} shifts when FC density varies in this case. When considering FC in the ungated zones of the HEMT (i.e. G-S or G-D zones), then I_{DSS} (and R_{ON}) changes as reported on g_m profiles versus V_{GS} in Fig. 12, whereas V_{th} remains constant. T-CAD simulations enable the FC effects at the interfaces of the #A gated zone to be differentiated from that in the #B ungated zones over the electrical behaviours before and after application of the stress.

The average 35% reduction on I_{DSS} is then achieved by simulation using a higher FC density in the ungated zone #B (increase by ΔFC=-1,2.10^{12} cm^{-2}). The sensitivity of V_{th} with fixed charge variation (ΔFC) is constant whatever the initial FC density, and equal to $\Delta V_{th}/\Delta FC$= 0.5.10^{-12} V/cm^{-2}. Then, simulations corroborate well with the measurements (featuring +0.2V to +0.5V increase in V_{th} after HTOL stress, i.e. 6% to 15% in Fig. 1), if using a fixed charge density variation ΔFC between 0,4.10^{12} cm^{-2} and 10^{12} cm^{-2}. It is also noticed a positive shift of V_{th} when performing transient measurements as evidenced in [7]. Different evolutions can be found for V_{th} in the literature: a drift towards more negative threshold values after stress periods is reported in [8], caused by substitutional and interstitial oxygen complexes but featuring recoverable effects due to the nature of these defects.

Two simulation plans are used as depicted in Fig. 10 (#A and #B); an average of ΔFC=10^{12} cm^{-2} variation in the density of fixed charge at the AlGaN/2DEG interface accounts both for the V_{th} shift and for the I_{DSS} reduction (first order G-S spacing and second order G-D spacing). Fixed Charges variation between gate and drain account for the R_{ON} increase. These results are consistent with some other papers, even if related to recoverable effects [10].

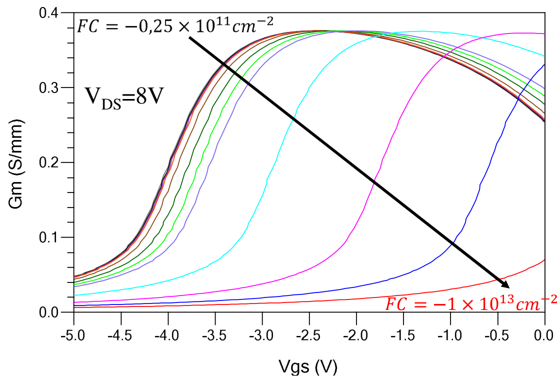


Fig. 11. Simulated transconductance gain with V_{DS}=8V for different fixed charges densities FC under the gate finger (case #A, negative FC at interface ③). FC ranges from -0,25.10^{11} cm^{-2} to -1.10^{11} cm^{-2} (step 0,25.10^{11} cm^{-2}), from -0,25.10^{12} cm^{-2} to -1.10^{12}cm^{-2} (step 0,25.10^{12} cm^{-2}) and from -0,25.10^{13} cm^{-2} to -1.10^{13}cm^{-2} (step 0,25.10^{13} cm^{-2}).

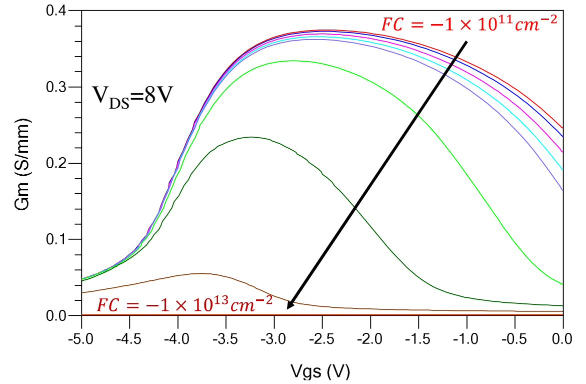


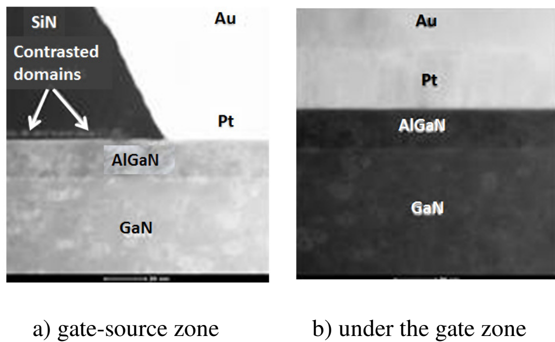
Fig. 12. Simulated transconductance gain with V_{DS}=8V for different fixed charges densities FC under the ungate G-S (G-D) zone(s) (case #B, negative FC at interface ③). FC ranges from -0,25.10^{11} cm^{-2} to -1.10^{11} cm^{-2} (step 0,25.10^{11} cm^{-2}), from -0,25.10^{12} cm^{-2} to -1.10^{12}cm^{-2} (step 0,25.10^{12} cm^{-2}) and from -0,25.10^{13} cm^{-2} to -1.10^{13}cm^{-2} (step 0,25.10^{13} cm^{-2})

4. Imaging with STEM HAADF and TEM lamella

TEM analysis gives a direct proof of structural defects in GaN structures, and has led to major issues for GaN technology improvements from different works, as in [9]. Next studies on STEM HAADF and TEM lamella have been driven by DGA MI (French MoD) on HTOL stressed devices.

4.1. Scanning Transmission Electron Microscopy High Angle Annular Dark Field (STEM-HAADF) – section view

STEM-HAADF images are suitable to define clearly the interface between GaN, AlGaN, SiN passivation layer or Gate Schottky metal; a FIB cut in the gate region allows an imaging of the stacked layers. Strong contrast can be identified between the layers as proposed in Fig. 13 a and b (respectively in the gate-passivation zone and under the gate metal). Contrasted domains are noticed at the interface between the passivation layer and the AlGaN layer. This 'unexpected' layer is constituted with Ga, Al and O species (by EDX and EFTEM), and is considered to be resistive. This observation is consistent with the highly resistive behavior at low I_{GS} (Fig. 8 and Fig. 9 inset).



a) gate-source zone b) under the gate zone

Fig. 13. STEM-HAADF images (FIB cut) performed by Biophy Research a) on the gate edge between gate and source and b) under the gate.

4.2. TEM lamella by removing the gate metallization - top view

TEM lamella of the gate foot (top view after removing the metallization of the gate finger) is reported in Fig. 14; the presence of voids under the gate finger is consistent with the inhomogeneity of the SBH revealed in Fig. 6 and Fig. 7.

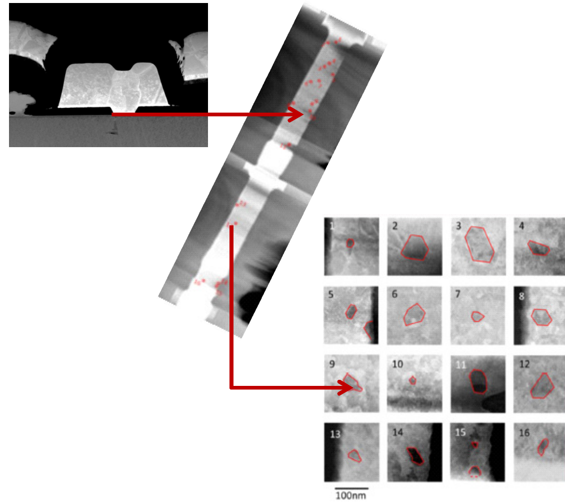


Fig. 14. TEM lamella of the gate finger (top view) performed by SERMA: identification of defects (voids) under the gate.

5. Conclusions

The identification of the impacting physical mechanism on the degradation of a (batch of) device(s) during the application of a stress is difficult to achieve. Usually, different contributors have to be considered together, but are not easily identifiable using a single method (experimental or simulation). Crossing dedicated measurements techniques and models with T-CAD simulations enlarges the field of investigation for failure analysis and process improvement. A failure analysis study case focused on gate Schottky diode inhomogeneity and interface states in the gated and ungated zones of the transistor have been presented.

It has been demonstrated the difficulty to achieve accurate Schottky Barrier Height extraction; the new proposed method accounts for the ideal SBH (extracted at 1.1eV), and also evidence different scattering processes on the SBH before and after the application of the HTOL stress.

From an electrical model developed at different temperatures, several gate current contributors have been extracted (evidencing two SBH paths); a focus was given on a highly resistive behavior occurring near the Thermionic Emission mode.

These results on the SBH inhomogeneity and on the highly resistive layer at the passivation/AlGaN interface corroborate with the different TEM analysis of the gate proposed in section view and top view.

T-CAD model has also been developed to assess the HTOL stress induced variations on I_{DSS} and on V_{th}.

Fixed charge density variations at the AlGaN/2DEG interface have been used in the gated zone and in the ungated zones of the modeled transistor to account respectively for the V_{th} drift and for the I_{DSS} reduction. Results also corroborate well with measurement considering the impact of $\Delta FC=10^{12}$ cm^{-2} on V_{th} and on I_{DSS} after combining the effects from each zone.

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