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Low-frequency noise in reverse-biased Schottky barriers on InAlN/AlN/GaN heterostructures

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We present low-frequency gate noise characteristics of InAlN/AlN/GaN heterostructures grown by low-pressure metal-organic vapor phase epitaxy. The electric field in the InAlN barrier is determined from C-V measurements and is used for gate leakage current modeling. The latter is dominated by Poole-Frenkel emission at low reverse bias and Fowler-Nordheim tunneling at high electric field. Several useful physical parameters are extracted from a gate leakage model including polarizations-induced field. The gate noise fluctuations are dominated by trapping-detrapping processes including discrete traps and two continuums of traps with distributed time constants. Burst noise with several levels and time constant values is also observed in these structures. Low-frequency noise measurements confirm the presence of field-assisted emission from trap states. The 1/*f* noise model of McWorther is used to explain the 1/*f*-like noise behavior in a restricted frequency range. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4901906]

InAlN/GaN high electron mobility transistors (HEMTs) are very promising devices for power amplification at microwave and millimeter wave frequencies.[1,2] The InAlN barrier provides high carrier density and can be well lattice matched (assuming 17% indium concentration) to the GaN buffer which is expected to improve the reliability of the device.[3] As pointed out by several authors,[4–6] the gate leakage current remains a limiting factor, and the related physical mechanisms must be well understood to make the most of this technology. There is a lack of data related to their low-frequency noise characteristics in the literature, compared to the AlGaN/GaN heterostructure, which is probably due to the fact that this technology is currently under development. Low-frequency noise is sensitive to the presence of defects and impurities in semiconductors and can be advantageously used as a diagnostic tool to evaluate the quality and reliability of these electronic devices.[7] It is also a key parameter to realize low phase-noise circuits. We focus this paper on the low-frequency gate noise current in reverse-biased Schottky barrier realized on InAlN/AlN/GaN heterostructure. Both C-V and dc measurements are also used to highlight the impact of the strong electric field in the InAlN barrier on the noise characteristics.

The transistors used in this paper are grown by low-pressure metal-organic vapor phase epitaxy (LP-MOVPE) on an SiC substrate. The heterostructure consists of a 1.7-μm-thick GaN buffer, followed by a 1-nm-thick AlN spacer layer and a 10-nm-thick InAlN barrier layer with 21% of indium content. The sheet resistance and the sheet carrier density are 330 Ω/sq and $1.45 \times 10^{13}\,\mathrm{cm}^{-2}$, respectively. Rapid thermal annealing of Ti/Al/Ni/Au stacks at 900 °C under nitrogen atmosphere is used to form the ohmic contacts. Ni/Pt/Au T-gate is formed after electron beam lithography. The gate length is 0.15 μm, the total gate width is 150 μm, and the gate-source distance is 0.5 μm. The devices are passivated with a 250-nm-thick Si_3N_4 layer. The current gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{MAX}) are 40 GHz and 110 GHz, respectively. Very promising performances in terms of output power density have been measured at 18 GHz (12 W/mm) and 30 GHz (2.5 W/mm).[2] The minimum noise figure and associated gain at 20 GHz are 1.25 dB and 11 dB,[2] respectively, which are very close to the best results measured on similar transistors with smallest gate length.[8]

Figure 1 represents the variations of the gate current versus the applied gate voltage measured at 300 K when the drain is open-circuited. The forward current largely increases for gate voltage values higher than 1 V, while the reverse current tends to saturate for reverse voltage greater than 2.5 V. The inset in Figure 1 shows the forward gate current plotted in a logarithmic scale versus the gate voltage. The solid line corresponds to the classic expression of the thermionic current used to determine the barrier height ϕ_b and the ideality factor

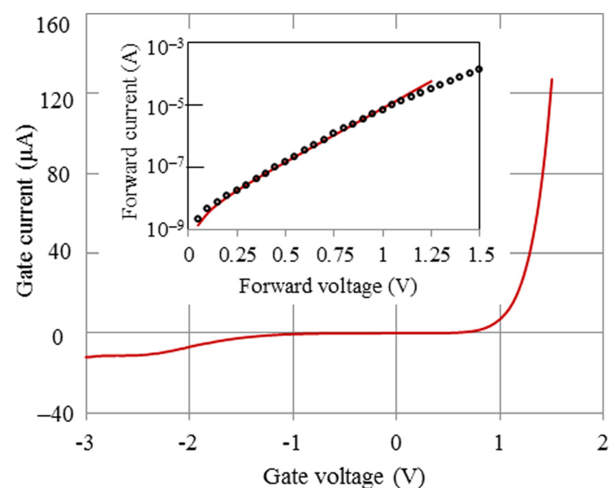

FIG. 1. Gate current versus gate voltage at 300 K. The inset represents the forward current versus forward voltage. Open circles correspond to measurement data. The solid line corresponds to the thermionic model.

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n of the Schottky contact. We have found that $\phi_b = 0.51$ eV (assuming that the Richardson constant is equal to 56 A/cm^2 K^2)[9] and $n = 4.9$. Measurements versus temperature has been made to extract the mean value of the barrier height $\overline{\O_b}$ and its standard deviation σ_s used in the model of Werner and Güttler.[10] We have found that $\overline{\O_b} = 0.85$ eV and $\sigma_s = 0.13$ eV. The behavior of the forward current needs an in-depth study to explain the high value of n and the deviation between the thermionic model and experimental data for gate voltage larger than 1 V. These preliminary results indicate the presence of barrier inhomogeneities in our structure probably due to the presence of surface states and/or interface defects as reported by others.[9] However, the main objective of this letter is to evaluate the low-frequency noise in reverse-biased Schottky barriers, corresponding to the bias conditions of InAlN/AlN/GaN HEMTs.

Figure 2 shows the gate leakage current as a function of the reverse gate voltage V_R measured at 300 K when the drain is open-circuited. The current rises as V_R increases and saturates at 2.5 V. A theoretical model including both Poole-Frenkel and Fowler-Nordheim components is also superimposed on the plot. The vertical component of the electric field F in the InAlN barrier is shown in the inset of Figure 2 and is determined from the Gauss theorem and C-V measurements using the following expression:

$$F = \frac{q(\sigma_{InAlN/AlN} + \sigma_{AlN/GaN} - n_s)}{\varepsilon_0 \varepsilon_r}, \quad (1)$$

where q is the electronic charge, ε_r is the low-frequency relative permittivity of the InAlN barrier equal to 11.2,[11] and ε_0 is the permittivity of free-space. $\sigma_{InAlN/AlN}$ and $\sigma_{AlN/GaN}$ are the interface polarization charges including both spontaneous and piezoelectric polarizations. The values are calculated using the expressions given by Ambacher *et al.*[11] and are equal to -4.7×10^{13} cm^{-2} for the InAlN/AlN interface and 6.8×10^{13} cm^{-2} for the AlN/GaN interface. n_s is the two-dimensional electron gas (2DEG) carrier density obtained by integration of the C-V plot. The vertical electric field can be represented by a linear expression $F = F_0 + V_R/d$ (dashed line in the inset of Figure 2) for reverse voltage values less than 1.5 V. F_0 represents the zero-bias field (1.06 MV/cm) and d is the thickness of the semiconductor ($d = 9.4$ nm, which is close to the barrier thickness value). The value of the saturation field is 3.35 MV/cm and occurs for V_R values above 2.5 V. The reverse gate current due to the Poole-Frenkel effect is given by[4]

$$I_{gPF} = C_{PF} F \exp\left(-\frac{q(\O_t - \sqrt{qF/\pi\varepsilon_0\varepsilon_s})}{kT}\right) - I_{gPF0}, \quad (2)$$

where C_{PF} is a constant, k is the Boltzmann's constant, T is the temperature, and ε_s is the high-frequency relative permittivity of the semiconductor. Φ_t is the barrier height for electron emission from trapped state. I_{gPF0} is the Poole-Frenkel gate current value at $V_R = 0$ to keep the net diode current equal to zero.[4,12] Measurements between 150 and 300 K have been made to extract the values of ε_s and Φ_t. We have found that $\varepsilon_s = 6$ and $\Phi_t = 0.1$ eV from the Arrhenius plots. The values of ε_s and Φ_t in our device agree with the previous results.[4,13–15] These results indicate that the leakage current is controlled at low reverse bias by emission of electrons from a trap state into a continuum of states associated with a conductive dislocation as suggested by others.[16] The reverse gate current is dominated by Fowler-Nordheim tunneling at high field. Due to the presence of a large polarization-induced electric field at zero bias, the classical expression of this tunneling current[17] is modified as follows:

$$I_{gFN} = C_{FN} F^2 \exp\left(-\frac{B}{F}\right) - I_{gFN0}, \quad (3)$$

with $C_{FN} = \frac{Aq^3}{8\pi h \O_b}$ and $B = \frac{8\pi}{3qh}\sqrt{2\O_b^3 m_t^*}$. A is the gate surface, h is the Planck's constant, Φ_b is the barrier height, and m_t^* is the electron tunneling effective mass in the InAlN barrier. I_{gFN0} is the zero-field current used to keep the diode current equal to zero at $V_R = 0$ V. We extract from our model that the barrier height to be $\Phi_b \sim 0.52$ eV (very close to the value determined from the forward biased characteristic shown in the inset of Figure 1), and the tunneling effective mass to be $m_t^* \sim 0.3\, m_e$.

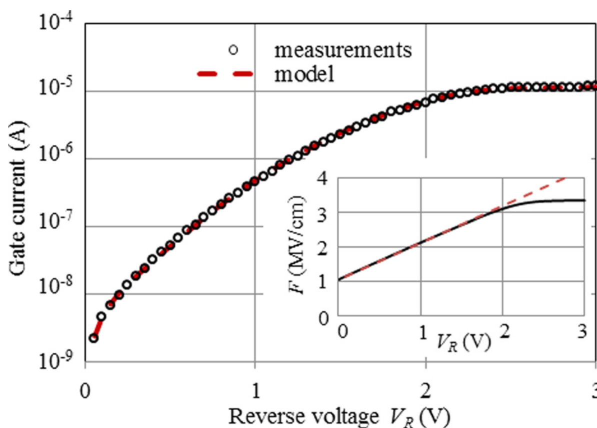

FIG. 2. Gate leakage current versus reverse voltage at 300 K. The inset (solid lines) represents the variations of the vertical electric field in the InAlN barrier determined from C-V measurements versus reverse bias voltage.

The low-frequency noise characteristics of the gate current, when the drain is open-circuited, are measured using a low-noise transimpedance amplifier and an FFT analyzer in the frequency range of 1 Hz–100 kHz. Measurements are made in a Faraday's shielding. An oscilloscope is also connected at the output of the amplifier to track the measured noise signal in the time domain. The noise contribution of both the bias circuitry and low noise amplifier is taken into account to determine the power spectral density (PSD) S_{ig} associated with the gate current fluctuations. The noise floor of the test set is less than 10^{-23} A^2/Hz, which is larger than the barrier shot noise. All the measurements are realized when the gate current is stable to avoid any drift during the noise characterization which is time consuming due to several frequency bands and large averaging. Figure 3 shows the PSD of the Schottky barrier measured for several values of the reverse voltage. We can observe that the noise level increases with V_R and tends to saturate for V_R values greater than 1.7 V. Additional measurement at $V_R = 3$ V (not shown in Figure 3) indicates fall-off of the noise level. This could

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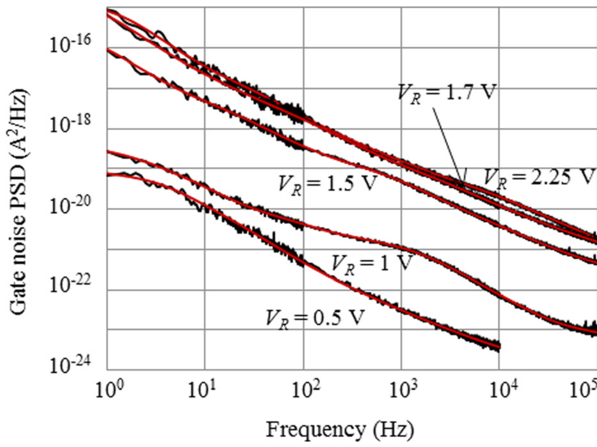

FIG. 3. Gate noise power spectral density versus frequency measured at 300 K. Dotted lines: model, thin solid lines: measurements.

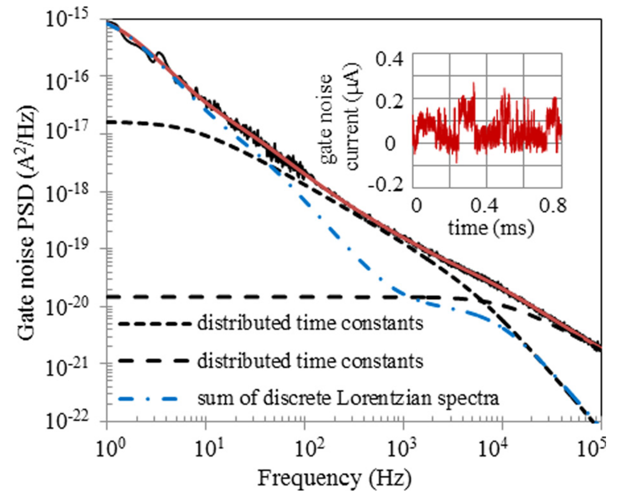

FIG. 4. Gate noise power spectral density versus frequency at $V_R = 2.25$ V showing the different components of the model. The inset represents the variations of the gate noise current in the time domain and clearly shows the presence of burst noise in the device.

be correlated with a decrease of the carrier number in the 2DEG and their associated noise. This behavior is different compared to the one of AlGaN/GaN devices[18,19] where a continuous increase of the noise level is observed when the reverse voltage grows. All the spectra are dominated by many Lorentzian components due to the presence of several traps behaving like recombination centers. Analytical models are also superimposed on the measured plots. Several discrete traps and two trapping-detrapping processes with distributed time constants are used to fit the measured data. The gate noise PSD is given by[20]

$$S_{ig} = \sum_{i=1}^{n} \frac{A_i \tau_i}{1 + (2\pi f \tau_i)^2} + \sum_{j=1}^{m} \frac{B_j [Arctg(2\pi f \tau_{j1}) - Arctg(2\pi f \tau_{j0})]}{f Ln(\tau_{j1}/\tau_{j0})}, \quad (4)$$

where f is the frequency, and A_i and τ_i are the amplitude and the time constant associated with the ith discrete trap, respectively. The second term in (4) is due to the presence of trapping-detrapping processes with distributed time constants in the interval $[\tau_{j0}\text{-}\tau_{j1}]$ and is used to describe a $1/f$ behavior of the spectrum in a restricted frequency range.[21] B_j is the amplitude of the jth noise process. Two distinct processes are used in our devices except for $V_R = 0.5$ V where only one process is necessary with time constants arbitrarily fixed to have a $1/f$ spectrum in the whole measured frequency range. The parameters of the model (A_i, τ_i, B_j, τ_{j0}, and τ_{j1}) are determined by plotting $f \times S_{ig}(f)$ versus frequency, which is commonly used to extract the main characteristics of noise spectra with equally weighted PSD versus frequency.[22] Figure 4 represents the different components of the model at $V_R = 2.25$ V. We observe a very good agreement between the calculated spectrum and experimental data. The choice of trapping-detrapping processes with distributed time constants is justified by the presence of burst noise or random telegraph signal (RTS) shown in the inset of Figure 4. We observe several levels with durations varying on a large scale. Another reason is found after an attentive inspection of the spectrum shown in Figure 4. We note a $1/f$-like noise behavior for frequencies above 10 kHz. A simple extrapolation toward lower frequencies should give a noise level greater than the measured data between 100 Hz and 10 kHz, which is obviously wrong. Only the spectrum given by the dashed line (a plateau followed by a $1/f$-like noise) allows an appropriate modeling of the measured values. Distributed time constants attributed to spatial fluctuations in the barrier height are also used by Kumar *et al.*[23] to explain the $1/f$ noise behavior in GaN diodes in the presence of barrier inhomogeneities. The latter point has been evidenced in our structure with dc measurements. $1/f$ noise due to mobility fluctuations[24] is not perceptible in our device since all the measured spectra are dominated by trapping-detrapping processes. The values of the time constants τ_{j0} and τ_{j1} vary with the applied bias and decrease when V_R grows. A possible explanation is the manifestation of Poole-Frenkel effect, but the analysis on the set of the extracted values does not definitively prove this assumption. Three or four discrete traps are also used in our devices depending on the investigated bias point. A trap with a time constant value of around 150 ms is found in our structure. Another one with a time constant less than 1 μs is also

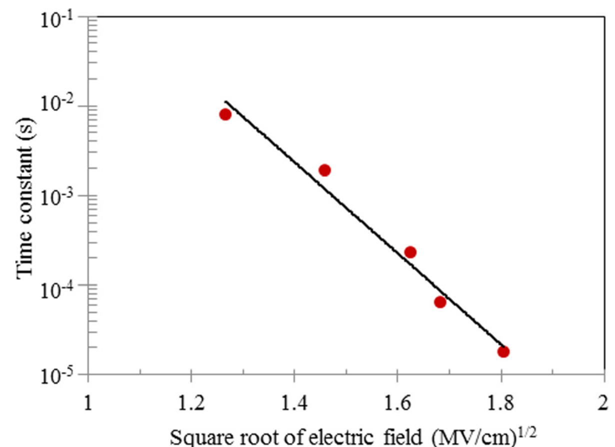

FIG. 5. Time constant of a discrete trap versus the square root of electric field. Solid line: exponential fit.

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used to fit the high-frequency part of the spectra. We have noted the presence of a discrete trap with a bias-dependent time constant. Figure 5 shows the variations of the extracted time constants versus the square root of the electric field. The solid line indicates that the logarithm of the time constant varies with $\sqrt{F}$ due to Poole-Frenkel effect. The trap potential barrier height can decrease due to the strong electric field in the InAlN barrier. The direct consequence is a reduction of the time constant of the trap equal to $\tau_0 \exp(-\alpha\sqrt{F})$.[25] τ_0 is a characteristic of the trap at zero field and α is equal to $\frac{1}{kT}\sqrt{q^3/\pi\varepsilon_0\varepsilon_s}$. The value of α is determined from the fit, and we found that ε_s is equal to 6.3, which is close to the value extracted from dc measurements.

In summary, we have studied the Schottky contact from both dc and low-frequency noise measurements on InAlN/AlN/GaN heterostructures. The main physical parameters of the Schottky barrier have been extracted from dc characteristics. Our results indicate the presence of barrier inhomogeneities probably due to the presence of surface states and/or interface defects. This assessment has also been evidenced with low-frequency noise measurements. The noise level in our structures is of the same order of magnitude compared to the results published on AlGaN/GaN devices[18,19] with approximately equivalent gate surface values. We have shown that the gate noise level decreases when the electric field saturates. This could be attributed to a reduction of the carrier number in the 2DEG interacting with traps in the GaN buffer or at the AlN/GaN interface. The noise is globally dominated by trapping-detrapping processes. Burst noise was also observed which could be due to dislocations as reported in the past in silicon bipolar transistors.[26] This assumption is coherent with the presence of Poole-Frenkel effect experimentally evidenced in both the dc characteristics and noise measurements. A noise modeling approach including trapping processes with distributed time constants has also been proposed. This could be due to electrons interacting by Fowler-Nordheim tunneling with traps located at the surface or at the metal semiconductor interface. This approach is in accordance with the small-signal modeling of InAlN/AlN/GaN HEMTs proposed by the authors in a previous paper.[27]

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