GaN Technologies: From The Improvement Of Device Reliability To The Design Of Robust High Frequency Circuits

Pr. Jean-Guy TARTARIN  
Professor  
LAAS-CNRS and University of Toulouse, University Paul Sabatier, France  
tartarin@laas.fr

Session 1-3: Terahertz Technologies and Microwave Technologies
WHAT IS MATERIAL ? WHAT IS A SYSTEM ? INTRODUCTORY PART...

For a physicist:

PHYSICS fundamental concepts (condensed matter) are used to develop new MATERIALS (gathering chemistry, solid state physics and mechanics) by description of their physical properties.

    outputs are concerning electronic, optical ‘SYSTEMS’ and much more (novel structures, ...)

Bridging the gap ! (bottom-up & top down strategies)

For an (High-Frequency) electrical engineer:

MATERIALS are used to process DEVICES (active /passive),

    DEVICES are used to design CIRCUITS (block functions)

    CIRCUITS are assembled to build (sub)-SYSTEMS...
OUTLINE OF THE PRESENTATION

-GaN technology

-GaN transistors:
a complex ‘system’ between materials & electrical worlds
(optimization and trade-offs)

-exploration of defects in GaN transistors (HEMT) – reliability at device level

  -destructive solutions to evidence defects, but... are these defects active?
  -non invasive measurement techniques, but... what is the cause ?

-impacts on (real situation) operating mode –reliability at circuit level

-conclusions and perpectives
OUTLINE OF THE PRESENTATION

-GaN technology

-GaN transistors: a complex ‘system’ between materials & electrical worlds (optimization and trade-offs)

-exploration of defects in GaN transistors (HEMT) – reliability at device level
  -destructive solutions to evidence defects, but... are these defects active?
  -non invasive measurement techniques, but... what is the cause?

-impacts on (real situation) operating mode – reliability at circuit level

-conclusions and perpectives
GaN TECHNOLOGY

- Advantages ...

- Lattice mismatch
- Thermal management
- High voltage fields
- PiezoElectr
- Leakage currents

... and Drawbacks

- partial or recoverable degradation mechanisms
- different time-dependant traps (from µs to few seconds)

Power 🎀 🎀 🎀 🎀 🎀 Freq. 🎀 🎀 🎀 🎀 🎀
Noise 🎀 🎀 🎀 🎀 🎀 to 🎀 🎀 🎀 🎀 🎀
Cost 🎀 🎀 🎀 🎀 🎀 to 🎀 🎀 🎀 🎀 🎀
Example of heterostructure for GaN on Si (111)
(also on SiC, Al₂O₃, GaN, diamond)

GaN TECHNOLOGY

- Mastering the technological steps:

  from material to the device and more!

As grown substrates characterized by AFM and ECCI


Largely inspired from Ref Hiramatsu et al. J. Crystall Growth 1991
### GaN TECHNOLOGY

#### -MBE vs MOCVD Advantages and drawbacks

<table>
<thead>
<tr>
<th>Growth technology</th>
<th>Strengths</th>
<th>Weaknesses</th>
<th>Frontier for 21st Century</th>
</tr>
</thead>
</table>
| Metal-organic chemical vapour deposition MOCVD MOVPE | - Well developed technology  
- Atomically sharp interfaces  
- In-situ thickness monitoring  
- High growth rates (<4 μm/hr)  
- Easily scalable for mass production  
- Short run cycles (heat+growth+cool)  
- Possibility to use plasma or laser assisted growth | - Lack of precise in-situ characterization  
- Large quantities of NH₃ are needed | Mass production of high quality III-Nitride thin films and devices |
| Molecular beam epitaxy MBE, GSMBE, MOMBE | - Well developed technology  
- Atomically sharp interfaces  
- Precise in-situ characterization  
- High purity growth environment  
- Hydrogen free environment  
- Scalable for mass production | - Need for ultra-high vacuum (cryogenics)  
- Long run cycles (heat+growth+cool)  
- Growth temperature is limited on the high end  
- Efficiency of nitrogen source or cracker (ECR, RF) is limited  
- Low growth rates (<1–1.5 μm/hr)  
- Not as high throughput as MOCVD | Growth in hydrogen-free environment |
| Vapor phase epitaxy VPE, HVPE | - Simple growth technique  
- Very high growth rate (<100 μm/hr)  
- Reasonably good quality films | - No sharp interfaces  
- Long run cycles (heat+growth+cool)  
- Small area growth  
< Better films are obtained for lower growth rates | Thick GaN films for substrates |
| High pressure growth | - Bulk GaN single crystals | - Only for GaN single crystals  
- Small size crystals (few mm² area)  
- Extreme temperature and pressure conditions | Bulk GaN single crystals for substrate use |
| Sublimation sandwich method SSM | - Very simple growth technique  
- Extremely high growth rate (<300 μm/hr) | - Poor quality of films  
- Need a GaN powder source  
- Small area growth | Bulk AlN single crystals for substrate use |
**GaN TECHNOLOGY**

-MBE vs MOCVD
Advantages and drawbacks (what is not given by bandgap engineering...)

**N-polar structure:** chemical abruptness is observed at the top interface between AlN and GaN, while the bottom interface between this pair of materials is diffuse. 

*Measurements were made of the three-dimensional distribution of gallium atoms from AlGaN/AlN/GaN heterostructures grown by:*
*plasma-assisted MBE with 2 nm interlayer (a) and MOCVD with 2 nm and 0.7 nm interlayer ((c) and (e), respectively)*

MOCVD-grown equivalent with an unintentional AlGaN interlayer is plagued by the combination of increased alloy disorder and interface roughness scattering, which both drag down 2DEG mobilities.

Ref: *Compoundsemiconductor, July 2013, Scrutinizing AlN-GaN heterostructures atom by atom*
- tradeoffs between bandgap engineering (lattice/thermal/electr. perf.) & reliability (induced defects)

Origin of the 2DEG, interface states and deep (border) discrete trap (T-CAD simulations)
Pinning effect, 2DHG formation, traps (lag and reliability)

Ref: Bakeroott et al. 2014 JAP

Using T-CAD software to calibrate a process and to bring it to maturity (translate physical processes and mechanisms into numerical 2D structure)
Cross experiments:

- non invasive techniques (I-V-T static and pulsed, [S] CW, pulsed, large-signal, ?-DLTS, TLS & EL,, Low Frequency Noise, nanostructural analysis by Raman spectr., OBIRCh ...)
- destructive techniques (FIB-cut, TEM & EDX, ...) ? (still uncertainty on the weight of the detected defects; DOES IT PLAY A ROLE IN THE FAILURE PROCESS ?)
- GaN technology

- GaN transistors: a complex ‘system’ between materials & electrical worlds (optimization and trade-offs)

- Exploration of defects in GaN transistors (HEMT) – reliability at device level
  - Destructive solutions to evidence defects, but... are these defects active?
  - Non invasive measurement techniques, but... what is the cause?

- Impacts on (real situation) operating mode – reliability at circuit level

- Conclusions and perspectives
GaN TRANSISTORS – HEMT
High Electron Mobility Transistors (Enhancement)/Depletion

-DEVICE OPTIMIZATION PROCESS TO QUALIFICATION (TRL 3 to 7)

Enhancement Depletion technologies → **Depletion for HF applications**

- Design and Process devices
- First (coarse) level measurements
  - static DC, RF [S], ft & fmax, Power(s)
  - refine process if needed
- Second (fine) level characterization
  - dedicated tools and workbenches
    (destructive TEM lamella, FIB cut, EDX… non destructive transient & harmonic meas., …)
- Through process qualification (reliability studies)

From http://www.ece.ust.hk/~ptc/research.php?action=EDHEMT
**GaN TRANSISTORS – HEMT**  
High Electron Mobility Transistors *(Enhancement)/Depletion*

**-MEASUREMENT RELIABILITY AND CONFIDENCE LEVEL FOR ROBUST ANALYSIS**

(ex: InAlN/GaN HEMT 0,25x2x75µm)

*Impact of detrapping processes at decreasing $V_{DS}$*

*Thermal @ increasing $V_{DS}$*

*Same behavior with $V_{GS}$ (increa./decreas.): impact of charges under the gated zone*

*Increasing $V_{DS}$ (different acquisition time)*

*Short 640µs, Medium 20ms, Long 320ms*
GaN TRANSISTORS – HEMT
High Electron Mobility Transistors (Enhancement)/Depletion

-ALSO T-CAD MODELS TO ASSESS MEASUREMENTS

g_m(V_{GS}) measured and simulated at different temperature (AlGaN/GaN HEMT)
**GaN TRANSISTORS – HEMT**

High Electron Mobility Transistors *(Enhancement)*/Depletion

- ALSO T-CAD MODELS TO ASSESS MEASUREMENTS

![Graphs showing measured and simulated $g_m(V_{GS})$ at different temperatures](image)

$g_m(V_{GS})$ measured and simulated at different temperature (AlGaN/GaN HEMT)
OUTLINE OF THE PRESENTATION

-GaN technology

-GaN transistors:
  a complex ‘system’ between materials & electrical worlds
  (optimization and trade-offs)

-exploration of defects in GaN transistors (HEMT) – reliability at device level

  -destructive solutions to evidence defects, but... are these defects active?
  -non invasive measurement techniques, but... what is the cause?

-impacts on (real situation) operating mode – reliability at circuit level

-conclusions and perspectives
- How can traps affect device characteristics?

- Directly trapping electrons in the channel (decreasing the 2DEG density): only buffer or AlGaN/GaN interface traps!

- Trapping charge out of the 2DEG, creating a change in the potential barrier to current flow (a virtual gate, spatially distinct from the metal gate)

- Trapping charge underneath the metal gate, effectively changing the gate bias. (pinch-off voltage changes, collapse should not depend on surface treatment) \( \Delta V_P = \frac{q \cdot \Delta n_s}{C_{AlGaN}} \)
-destructive solutions to evidence defects, but... are these defects active?

FIB cut, EDX chemical mapping, TEM lamella,…

Validation of hypothesis from non-invasive techniques by destructive EDX charac

-non invasive measurement techniques, but... what is the cause?

1. electrical characterization (DC & pulsed, DLTS, ...)
2. harmonic and transient studies, a large variety of dedicated tools!

Need a precise and robust procedure to make reliable comparisons and studies (attend O. LAZAR’ speech, young investigators forum on Wednesday)
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-Low Frequency Noise Measurements: fluctuations are attributed to crystal quality or defects (metal contact, passivation layers, doping & chemical structure modification... GR centers).

-Tests plans to evidence and locate defects within the device’ layers

✓ constant $V_{GS}$, $V_{DS}$, $V_{DG}$ to keep $n_i$, SCR between G-D or G-S constant for example)

✓ Temperature change

✓ Before/after application of stress (thermal, electrical, RF)
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-Low Frequency Noise Measurements $S_{IG}$ : modelling of spectra, extraction GR centers

$$S_{IG} = \sum_{i=1}^{n} \frac{A_i \tau_i}{1 + (2\pi f \tau_i)^2} + \sum_{j=1}^{m} B_j \left[ \text{Arctg}(2\pi f \tau_{j1}) - \text{Arctg}(2\pi f \tau_{j0}) \right] \frac{f \ln(\tau_{j1}/\tau_{j0})}{\tau_{j0}}$$

G-R

Distributed trapping process

3 to 4 G-R centers + distributed processes (contribution to the theory developped by Mc Worther)

Ref. N’Sele, JG Tartarin, L. Escotte, EDL 2014
DEFECTS IN GaN HEMTS: RELIABILITY @ DEVICE LEVEL

-Low Frequency Noise Measurements $S_{ID}$: GR evolution during stresses

Surface and AlGaN/GaN interface states
Solutions to remove defects (interlayer, cleaning, in-situ passivation)
DEFECTS IN GaN HEMTS: RELIABILITY @ DEVICE LEVEL

- transient measurements, and other electrical procedures

![Graphs and diagrams illustrating transient measurements and electrical procedures in GaN HEMTs.]

Intrinsic charges under the gate affect simultaneously $I_{DS}$-$I_{GS}$ with large time constant ranging.

2DEG effective biasing

Out of the DUT

Gate terminal potential

$V_{GS}$-intrinsic (fixed value by external SMU)

$V_{chances}$ (time): impact of charges

$V_{GS}$-intrinsic ($t$) = $V_{GS}$-intrinsic - $V_{chances}$ ($t$) (effective time dependent biasing voltage)

Source terminal potential (mass)

Into the DUT

$V_{DS}$-intrinsic

$V_{GS}$-extrinsic

$V_{DS}$-extrinsic

$V_{GS}$-extrinsic

$V_{DS}$-extrinsic

S

G

D

AlGaN

2DEG

GaN

Time varying charges (SCR)

V$_{chances}$ (time)
-10 GHz CW stresses on 0.25x2x75μm² AlGaN/GaN devices

\[ P_{\text{out}} \] and DC evolutions with time due to charges

\[ I_{\text{DS}} \] decrease not correlated to permanent degradation: investigation on origin of change in device control mechanisms (gate)

RF stress = reduction of \( n_i \) in the 2DEG but recoverable effect (charges)

Recovery by positive DC bias or by illumination
DEFECTS IN GaN HEMTS: RELIABILITY @ DEVICE LEVEL

- stress under thermal, DC (HTRB, HTOL, ...) and RF stresses

Evolution of $P_S(P_E)$, $V_{TH}$, $g_m$

@10 GHz

$g_m$ also confirmed by T-CAD simulations by changing barrier height (does not affect $V_{th}$)
GaN TRANSISTORS – HEMT
High Electron Mobility Transistors (Enhancement)/Depletion

- Electrical characterization (DC and dynamic – transient; RF linear; RF power)

For a given application: High Power Amplifiers, Robust Low Noise Amplifiers, High purity oscillator, DC-DC converters, switches, ...

This is what is used by circuit designers

MAKE A BRIDGE BETWEEN TECHNOLOGY AND SYSTEM
- GaN technology

- GaN transistors:
a complex ‘system’ between materials & electrical worlds
(optimization and trade-offs)

- exploration of defects in GaN transistors (HEMT) – reliability at device level
  - destructive solutions to evidence defects, but... are these defects active?
  - non invasive measurement techniques, but... what is the cause?

- impacts on (real situation) operating mode – reliability at circuit level

- conclusions and perpectives
- circuit design and stress
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-stress of (devices) CIRCUITS : Low Noise Amplifiers or Power Amplifiers

\[ P_{\text{OUT\_Power Amplifier\_GaN}} @11,2 \text{ GHz (thermal cycling -40°C / +90°C)} \]

Memory Effects & traps
DC quiescent point drift
RF output power drift
P1dB change

...
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-stress of (devices) CIRCUITS : Low Noise Amplifiers or Power Amplifiers

\[ P_{\text{OUT\_Power Amplifier\_GaN}} @11.2 \text{ GHz} (\text{thermal cycling} \ -40^\circ\text{C} / +90^\circ\text{C}) \]

Memory Effects & traps
DC quiescent point drift
RF output power drift
P1dB change
...
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-stress of (devices) CIRCUITS : Low Noise Amplifiers or Power Amplifiers

$P_{\text{OUT\_Power\_Amplifier\_GaN}} @11.2$ GHz (thermal cycling $-40^\circ\text{C} / +90^\circ\text{C}$)
DEFECTS IN GaN HEMTS: RELIABILITY @ DEVICE LEVEL

-stress of (devices) CIRCUITS: Low Noise Amplifiers or Power Amplifiers

\[ P_{\text{OUT\_Power Amplifier\_GaN}} @11.2 \text{ GHz (thermal cycling -40°C / +90°C)} \]
-stress of (devices) CIRCUITS: Low Noise Amplifiers or Power Amplifiers

$P_{\text{OUT\_Power Amplifier\_GaN}}$ @11.2 GHz (thermal cycling -40°C / +90°C)
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

-stress of (devices) CIRCUITS : Low Noise Amplifiers or Power Amplifiers

\[ P_{\text{OUT\_Power Amplifier\_GaN}} @11.2 \text{ GHz (thermal cycling -40°C / +90°C)} \]
-stress of (devices) CIRCUITS : Low Noise Amplifiers or Power Amplifiers

$P_{\text{OUT\_Power Amplifier\_GaN}}$ @11.2 GHz (thermal cycling -40°C / +90°C)
DEFECTS IN GaN HEMTS : RELIABILITY @ DEVICE LEVEL

- stress of (devices) CIRCUITS : Oscillators

**10 GHz oscillator**

$P_{out}$ and DC conditions are stable: Phase noise degrades by $+15\text{dBc/Hz}$ (charges)

**30 GHz LNA**

$P_{1\text{dB}}$ degrades with CW stress. NF degrades under large input power (NL HF noise)
OUTLINE OF THE PRESENTATION

-GaN technology

-GaN transistors:
a complex ‘system’ between materials & electrical worlds
(optimization and trade-offs)

-exploration of defects in GaN transistors (HEMT) – reliability at device level
  -destructive solutions to evidence defects, but... are these defects active?
  -non invasive measurement techniques, but... what is the cause?

-impacts on (real situation) operating mode – reliability at circuit level

-conclusions and perspectives
TRADE OFFS between material-circuit-system; global approach to master each step

**Material properties**
- Wide bandgap
- High electron mobility
- High thermal conductivity

**Device properties**
- High power
- High frequency
- High yielding
- Elevated temperature

**SYSTEM LEVEL (architecture refinement)**
- HPA
- LNA
- VCO
- Mixer
- Switch

MAKE ALL REQUIREMENT MEET TO FULLY OPTIMIZE GaN TECHNOLOGIES
The final goal of the model is to:

- setup a physical model to optimize the technology (process and material, sizing of the device is connected to an understanding of the failure mechanisms and reliability aspect of device and circuit design)

- design robust RF circuits (smoother design, identification of unacceptable design limits or points of possible perf. losses with time).