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New Technological advances for microshielded coplanar circuits on silicon

E. Saint-Etienne*, G. Blasquez*, P. Pons*, R. Plana*, C. Douziech*,
P. Favaro*, Ph. Menini*, N. Fabre*, J. Graffeuil*, T. Parra* and J.C. Lalaurie**

Contact : G. Blasquez, blasquez@laas.fr, fax : (33) 561 33 62 08

* LAAS-CNRS, 7 Avenue du Colonel Roche 31077 Toulouse Cedex 4

** CNES, 18 Avenue Edouard Belin 31400 Toulouse

SUMMARY

An advanced technological process for microwave coplanar circuits on silicon oxide/nitride membrane is presented. This process allows to make thick conductors with high geometric definition. Furthermore, it permits to realise microshielded circuits with minimised losses in the access ports.

Keywords : Silicon ; technology ; microwaves

1. Introduction

In the course of the last decade, the feasibility of circuits on dielectric membrane has been demonstrated [1]. The potential domain of application of this technology encompasses centimeter and millimeter waves. Along the line of works previously initiated at the University of Michigan, we are developing since 1995 an optimised process where the membrane is made of a double layer of silicon oxide and silicon nitride. This process increases the production yield and minimises the manufacturing dispersion.

In 1998, we have developed new improvements which give the circuits a protection from mechanical damages, minimise electromagnetic interferences and reduce losses in the access ports.

2. The 1996 Issue

The original process technology [2] includes three main stages :

a) dielectric film manufacturing, by thermal oxidation of the silicon wafer, and LPCVD deposition of silicon rich silicon-nitride,

b) conductor manufacturing by photolithography or by local electrochemical deposition within a photoresist mould, the latter process being appropriate for thick conductors,
c) anisotropic etching of the silicon wafer under the conductors.

In this issue, mechanical and thermomechanical stresses have been minimised. It gives the devices a high stability throughout a wide range of temperature.

Demonstrators of coplanar transmission lines and filters on membranes of $1.4 \mu\text{m} \times 5 \text{ mm} \times 10 \text{ mm}$ have been manufactured from $\text{Ø}10 \text{ cm}$ wafers, with a production yield near 100%. The loss factor per unit length is less than 0.1 dB/mm in the frequency range 1-65 GHz.

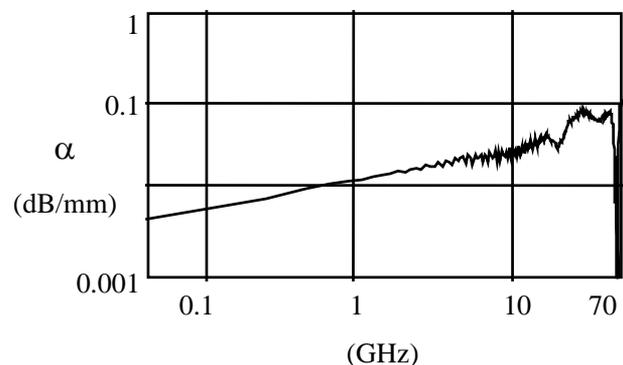


Figure 1 : Loss factor per unit length of a 75Ω transmission line on membrane

3. The 1998 Issue

3.1 Microshielding of the circuits.

The 1998 Issue of the technological process [3] allows to manufacture shields which protect the coplanar circuits from casual mechanical damages and prevents them from interaction with the electromagnetic environment and/or adjacent circuits. In other respects, the addition of shields increases the structural rigidity and makes the wafer slicing easier, whatever the operation is made, by cleaving or by sawing.

Shield manufacturing from silicon wafers includes :

- the deposition of an unalterable film used as an etching mask,
- the structuration of silicon wafers by chemical micromachining,
- the metallisation of the surface. Materials, equipment and processes used to make shields are identical with those used to make circuits.

Figure 2 shows eight covers in a perspective view. One can see the bridge, with windows on both sides for testing. Also visible are assembling wells used to join the circuit (here a bandpass filter) and the microshield cover.

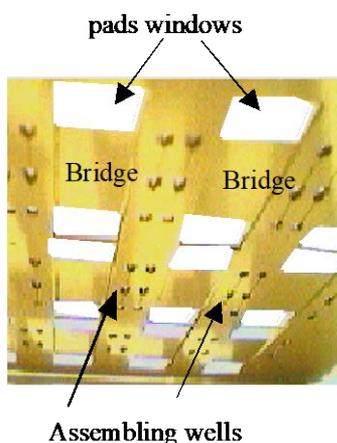


Figure 2 : Microshields shown from below

Figure 3 shows two microwave filters on membrane before and after integration of shields.

The total height of a microshielded filter is between 500 μm and 1 mm.

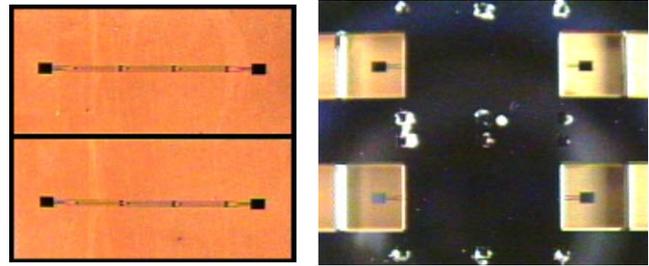


Figure 3 : Two bandpass filters shown before and after shielding

Figure 4 illustrates the transmission factor of a bandpass filter tuned at 30 GHz, without shielding and with shields 55 μm or 210 μm high. One can see that shielding reduces the bandwidth but does not modify the central frequency.

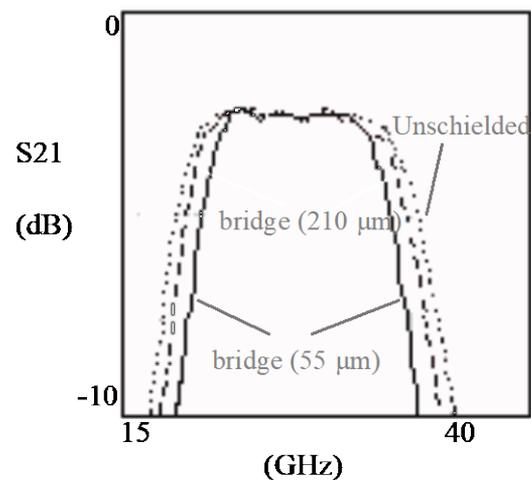


Figure 4 : Transmission factor of a bandpass filter with and without shield (bridge height 210 or 55 μm)

In order to produce microshielded coplanar circuits with a good accuracy, it appears necessary to control accurately the shield height. Silicon micromachining fulfills that condition. In other respects, as the wafers used to manufacture and the shield are both made of silicon, there is no differential thermal expansion. As a consequence, such microshielded circuits are able to operate in a wide range of temperature.

3.2 Improvement of the access ports.

The 1998 Issue of the process includes another improvement : the dielectric losses in the access ports are considerably reduced [4]. In the 1996 developments, the silicon wafer was not micromachined in the portions located under the access ports in order to operate on-wafer probing without any risk of damaging membranes. Circuit losses appeared to be almost totally located in these portions. They were already reduced by using high resistivity silicon and reducing the size of the access ports.

In the 1998 process, the dielectric film has been removed from the wafer in region of the access ports. In that way the conductors lie directly on the wafer and the Schottky junction enhances circuit insulation. Such phenomenon has already been reported in [5]. In order to validate that operating mode, two transmission lines 6 mm long have been manufactured on non micromachined wafers, one where the conductors were laid down on uncovered wafer, the other on wafer covered with the oxide/nitride film.

Figure 5 shows the loss factor per unit length obtained in both cases. Removing the film reduces the loss factor by a factor of 5 to 10 in the band 1-70 GHz. So the loss factor in the access ports at 50 Ω will be less than 0.2 dB/mm in that band.

Including this new improvements, the process is now composed of four main stages :

- a) dielectric film deposition,
- b) local etching of the film in the access ports,
- c) conductor formation,
- d) etching of the silicon wafer under the central part of the circuit.

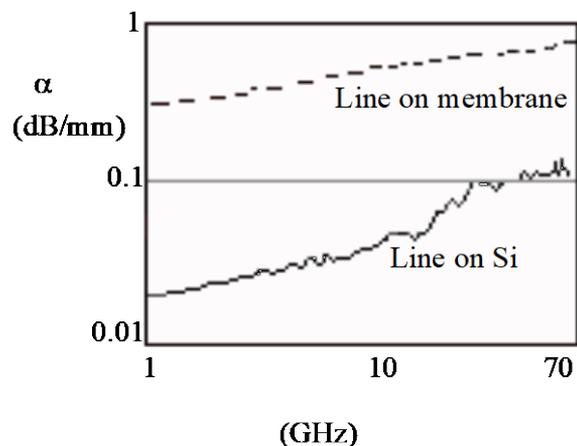


Figure 5 : Loss factor per unit length of two 50 Ω transmission lines, one on bare wafer, the other on wafer covered with the silicon oxide and nitride films.

References

- [1] L.P.B. Katehi ; Proc. IEEE, vol. 80, n°11, p 1771-1787, November 1992.
- [2] E. Saint-Etienne, and al ; Dixièmes Journées Nationales Micro-ondes ; Saint-Malo, p 212-213, Mai 1997.
- [3] E. Saint-Etienne, and al ; Sensors and Actuators – A ; vol. 68 / 1-3, p 435-441, 1998.
- [4] E. Saint-Etienne ; Doctorat de l'Université de Toulouse III ; November 1998.
- [5] A.C. Reyes, et al ; IEEE Transactions on MTT vol. 43, n°9, p2016-2022, September 1995.