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***Abstract* - In this study, forward and reverse conduction of SiC MOSFETs are characterized. These measurements allow us to demonstrate that forward and reverse output characteristics are different, while this was not taken into account in the SPICE model provided by die manufacturers. The difference is due to the body effect within SiC MOSFET and to the shift in threshold voltage. The threshold voltage was characterized as a function of the drain-source voltage V_{DS}. It is shown that V_{TH} decreases a lot when V_{DS} has greater negative values.**

I. INTRODUCTION

Within power device market, Silicon (Si) devices are used in most applications. However, these devices met their limits in many applications under harsh conditions. That is why researchers have put a great amount of effort into finding a new generation of power devices. The wide bandgap materials, like Silicon Carbide (SiC) or Gallium Nitride (GaN), are the most promising for high voltage, high temperature and high frequency applications [1].

In comparison to Si power devices, SiC equivalences offer a lot of advantages because of SiC material's intrinsic characteristics [1,2,3]. Silicon Carbide power devices, especially SiC MOSFETs and SiC Schottky diodes, have been growing fast in recent years. A great number of works were carried out in order to study behaviors of SiC MOSFET. Nowadays, most of SiC-based power device manufacturers provide electrical models (SPICE) for their components.

A good understanding of SiC MOSFET physics is important to accurately model these devices. The SiC MOSFET body diode has been subject of numerous researches. It was demonstrated that the body diode of SiC MOSFETs behaves differently compared to their Si counterparts [1], [4], [5]. This was firstly noticed by simulation [1] when the body diode current path goes through the channel and bypasses the p-n junction. The conduction capability of the body diode depends on gate-source voltage V_{GS} (0V to -5V) [5]. This is due to the body effect in SiC MOSFETs [5]. The change of threshold voltage in forward conduction mode was referred as drain-induced barrier lowering (DBIL) - a short-channel effect in MOSFETs [6]. However, this was not studied under negative V_{DS}.

In this work, forward and reverse conduction modes of SiC MOSFETs are characterized when the gate bias is positive. A difference between these output characteristics of SiC MOSFETs under these two conduction modes was found even when the body diode was not active. The phenomenon might be explained by the body effect within SiC MOSFET. Under reverse conduction, the drain bias is negative. The drop voltage between the gate and the top of drift region is positive which reduces the SiC MOSFET threshold voltage. In order to better understand the mechanism of MOSFET under these conduction modes, the threshold voltage V_{TH} is characterized as a function of drain-source voltage V_{DS} under forward and reverse conduction.

The results showed that under reverse bias, when V_{DS} takes a larger negative value (from -0,2V to -1,5V), the threshold voltage V_{TH} decreases rapidly (from 4,4V to -0,2V respectively). This change of the threshold voltage V_{TH} makes the MOSFET channel become more conductive in reverse conduction. On the other hand, under forward bias, the threshold voltage is almost invariant when the drain-source voltage V_{DS} changes.

The variation of the threshold voltage with the drain-source voltage will be modified in the electrical model. The results of modified simulation shows that the difference between forward and reverse output characteristics is most likely taken into consideration.

II. COMPARISON BETWEEN CONDUCTION MODES OF SIC MOSFET

In this section, the SiC MOSFET channel forward and reverse output characteristics are characterized using the curve tracer HP4142 under the following conditions:

- Gate-source voltage V_{GS} = 14-20V, drain current I_{DS} = 0-10A (forward conduction)
- Gate-source voltage V_{GS} = 14-20V, drain current I_{SD} = 0-10A (reverse conduction)

All the measurements are realized at ambient temperature (25°C). Fig. 1 illustrates the measurement circuit for each conduction mode.

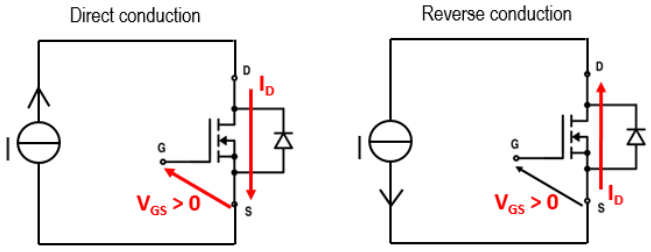

Fig. 1. Measurement circuit of SiC MOSFETs: forward (direct) conduction and reverse conduction.

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In order to compare the forward and reverse output characteristics of SiC MOSFETs, the absolute values of V_{SD} and I_D and the value of V_{DS} and I_D are presented in the same graph (see fig. 2).

As we can see in fig. 2, the drain-source voltage V_{DS} of SiC MOSFET in forward conduction is always higher than the reverse conduction one. When the gate bias is nominal (V_{GS} = 20V), there is still a significant difference between drain-source voltages V_{DS} of SiC MOSFET in these two conduction modes. Concretely, the values of drop voltage of the MOSFET under forward conduction and reverse conduction are 0.64V and 0.52V respectively at I_D = 10A, which means the on-state resistance of SiC MOSFET in forward conduction is about 20% higher than the reverse conduction one. This difference even becomes more significant when the gate bias voltage V_{GS} is lower. For example, at a gate-source voltage V_{GS} = 16V, the MOSFET drop voltages under forward and reverse conduction are 0.7V and 1.1V respectively (at drain current I_D = 10A). This means the on-state resistance of SiC MOSFET in forward conduction is 50% higher than the reverse conduction one. The ratio of the on-state resistance under these conduction modes is even closed to 2 at gate-source voltage V_{GS} = 14V.

This difference between SiC MOSFET forward and reverse output characteristics has not been yet taken into account in its electrical SPICE model provided by die manufacturers.

Fig. 3 presents the simulation output characteristics under the same conditions (V_{GS} = 14-20V, I_D = 0-10A) using the SiC MOSFET SPICE model. There is almost no difference between the simulation forward and reverse output characteristics at all range of the gate-source voltage V_{GS} (14V-20V).

At first, one might suppose that the conduction of the MOSFET body diode makes the drop voltage smaller in the case of MOSFET reverse conduction. However, at this small drop voltage (0.5V-1V), the body diode is not conductive yet (see fig. 4). Indeed, the body diode only starts conducting at a drop voltage 1.3V as illustrating in fig.4. This means, in both cases, the drain current goes through the MOSFET channel completely.

This phenomenon might be explained using short-channel effects in MOSFETs. When a bias voltage, which is higher than a certain threshold voltage V_{TH}, is applied between the gate and the source terminals, charges are induced in the interface layer of the semiconductor (also called the inversion layer). The threshold voltage V_{TH} represents the potential energy barrier against carrier injection from source to channel.

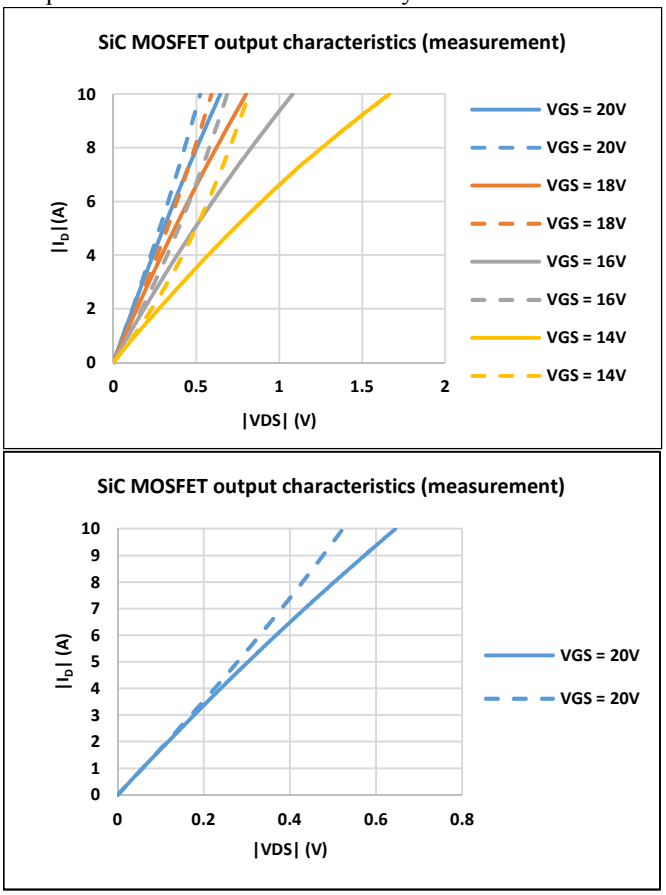

Fig. 2. Comparison of measurement forward and reverse output characteristics of STM SiC MOSFET (SCT50N120) under the gate bias voltage V_{GS} = 14-20V and a zoom for V_{GS} = 20V (reverse conduction as dashed line, forward conduction as continue line).

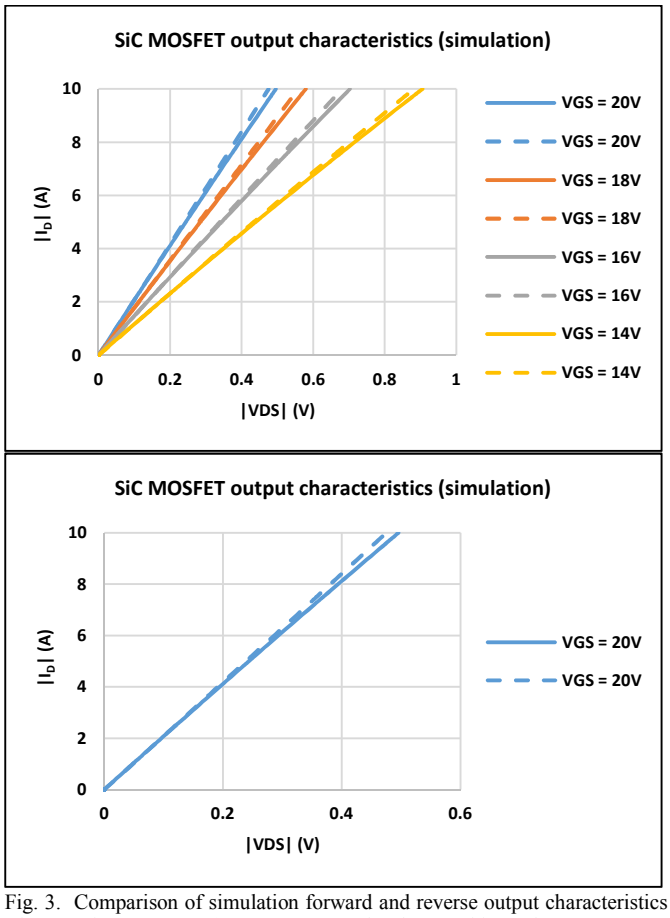

Fig. 3. Comparison of simulation forward and reverse output characteristics of STM SiC MOSFET (SCT50N120) under the gate bias voltage V_{GS} = 14-20V and a zoom for V_{GS} = 20V (reverse conduction as dashed line, forward conduction as continue line).

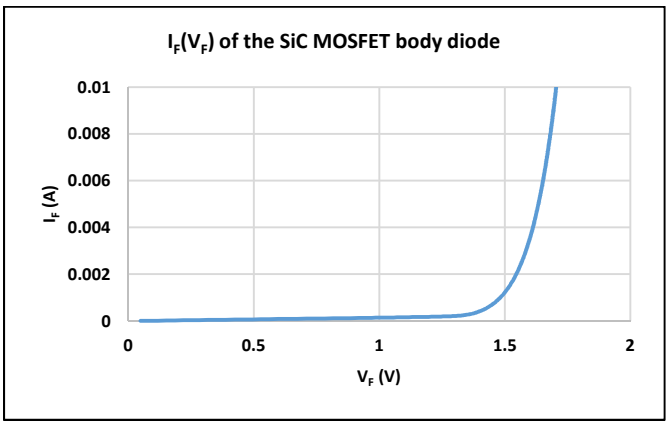

Fig. 4. $I_F(V_F)$ characteristics of the SiC MOSFET body diode (V_{GS} = 0V)

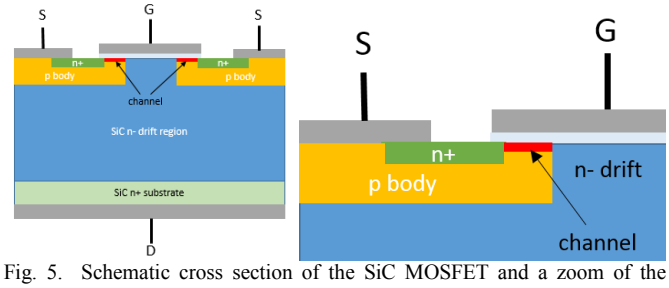

Fig. 5. Schematic cross section of the SiC MOSFET and a zoom of the channel.

Without any bias of the gate, when the drain-source voltage V_{DS} is negative, the voltage drop between the gate and the drift region V_{GD} is positive (fig. 5). This lowers the potential barrier and so reduces the threshold voltage V_{TH}. This mean, the channel will become conductive with smaller threshold voltage.

Fig. 6 presents the variation of $I_D(V_{DS})$ with different positive and negative drain-source voltages V_{DS}. The threshold voltage V_{TH} is define here as the minimum value of the gate-source voltage at a given drain-source voltage V_{DS} that allows a drain current of 1mA across the MOSFET.

As we can see in fig. 6, in forward conduction mode, the threshold voltage V_{TH} = 3,8V at V_{DS} = 0,5V. However under reverse conduction mode, the threshold voltage V_{TH} = 2,5V at V_{DS} = -0,5V.

According to the Shockley MOSFET equation that was used in the SiC MOSFET SPICE model, in linear region, the MOSFET drain current is the following:

$$I_{DS} = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS}) \qquad (1)$$

Where:

λ is the channel length modulation parameter,

μ_n is the charge carrier effective mobility,

C_{OX} is the gate oxide capacitance per unit,

W and L are the gate width and length respectively.

In the original model, the threshold voltage is represented as a constant to variation of the drain-source voltage. While this might be true for the case of forward conduction (V_{DS} > 0V), it is no longer true for reverse conduction. Indeed, as one

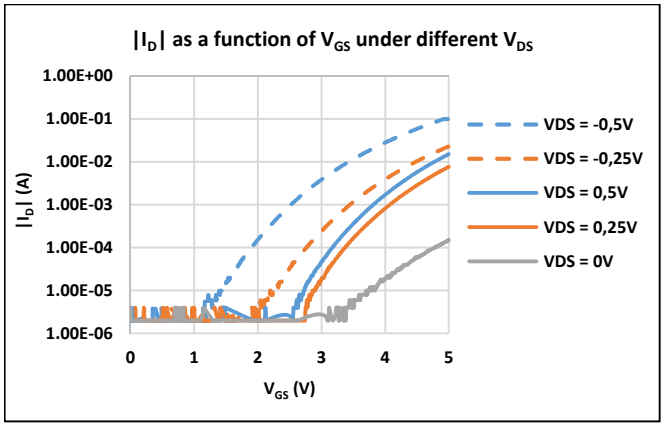

Fig. 6. Transfer characteristics of SiC MOSFET (in logarithmic scale) under different drain-source voltages

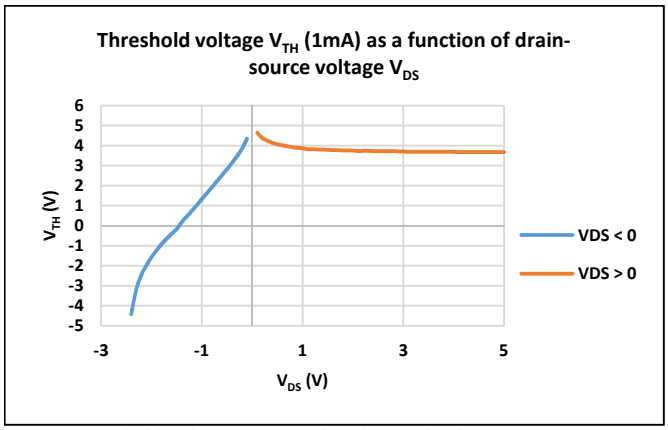

Fig. 7. Threshold voltage V_{TH} as a function of the drain-source voltage V_{DS} (here, the threshold voltage is defined as the minimum value of the gate bias voltage that allows a current of 1mA accros the MOSFET at a fixed drain-source voltage).

cans see in fig. 7, the threshold voltage decreases drastically when the drain-source becomes negative.

The threshold voltage continues to decrease when V_{DS} becomes more negative (from 0 to -1,5V) because of the body effect.

The threshold voltage V_{TH} has to be presented as a function of V_{DS} in order to accurately model I-V characteristics of SiC MOSFET.

Finally, in order to see the impact of the dependence of the threshold voltage V_{TH} – the drain-source voltage V_{DS} on simulation reverse output characteristics, several modifications have been made in the model. The threshold voltage is now a function of the drain-source voltage:

$$V_{TH} = f(V_{DS}) \qquad (2)$$

Fig. 8 illustrates the modified simulation forward and reverse output characteristics of SiC MOSFETs. The measurement characteristics are also added in this figure for comparison. As we can see, the modified simulation SiC MOSFET output characteristics takes into account the difference between forward voltage and reverse voltage. The simulation now accurately represents measurement characteristics.

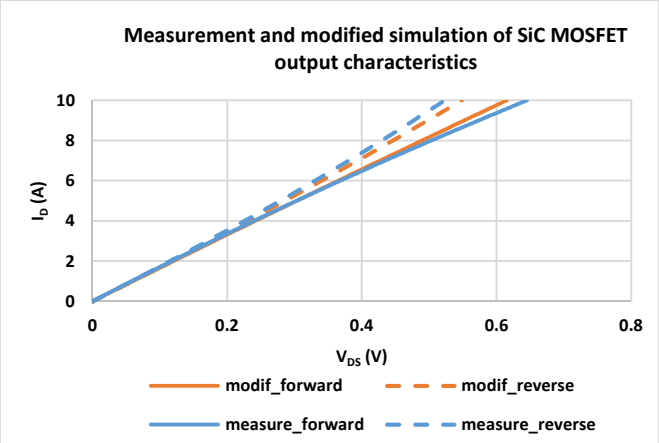

Fig. 8. Measurement and modified simulation of SiC MOSFET output characteristics (V_{GS} = 20V).

III. CONCLUSION

Forward and reverse conductions of SiC MOSFETs are characterized under varying positive gate bias voltages. It is demonstrated that SiC MOSFET reverse conduction capability is better than its forward conduction capability. When the gate-source voltage V_{GS} is nominal, under the same drain current, the MOSFET forward drop voltage is about 20% higher than its reverse drop voltage. The difference is even more accentuated with lower gate-source voltage.

Because of the body effect, a shift in the threshold voltage happens due to the reverse bias. The threshold voltage V_{TH} varies a lot when drain-source voltage V_{DS} is negative. Concretely, during reverse conduction mode, when the drain-source voltage V_{DS} has a larger negative, the threshold voltage V_{TH} decreases. This reduction of the threshold voltage makes the MOSFET channel become more conductive under reverse bias. The dependency of V_{TH} as a function of V_{DS} has to be taken into account for SPICE modeling of SiC MOSFETs.

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