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Preliminary Study on the Impact of Place and Route Strategy on FPGA Electromagnetic Emission

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Invited Paper

***Abstract* — Dense integration and high operating frequencies associated with increased number of I/O buffers of FPGAs are factors contributing to electromagnetic emission (EME) increase. Consequently the radiation issue that used to be discussed at PCB level has shifted to component level. Thus it is of high interest and challenging to investigate chip electromagnetic performance. This paper presents a preliminary analysis about the impact of the placement and routing (P&R) process of logic inside the FPGA on the chip EME level. With this purpose, a softcore processor was placed and routed based on three different strategies in the configurable logic block (CLB) array of a commercial FPGA and executed an application code running over an operating system (OS). Three experiments based on far- and near-field emission measurements have been performed.-The obtained results indicate that the EME level can be affected up to 21.8% by the way the processor is placed and routed inside the FPGA.**

Keywords — Commercial Field-Programmable Gate Array (FPGA), Reliability, Logic place and route process, Electromagnetic emission (EME), GTEM Cell Test Method, Surface Scan Test Method.

I. INTRODUCTION

As semiconductor technologies have been shrinking, the speed of circuits, integration density, and the number of I/O interfaces have been significantly increased. As consequence, electromagnetic emission (EME) became a paramount issue in the integrated circuit (IC) design. In this scenario, engineers must guarantee the ability of electronic components to operate safely in an increasingly hostile electromagnetic environment. Therefore, dealing to better understand the relationship between ICs and EME, several studies have been found in the literature dealing to define measurement procedures and standards, laboratory setup and countermeasures to understand and minimize EME from ICs. King Lee Chua *at al.* [1] presented an alternative approach to measure electromagnetic emissions by locating the entire FPGA test board inside the GTEM cell instead of mounting it at the wall of the cell. In [2], authors evaluate and analyze the impact of I/O switching activities on the EME of a Xilinx Spartan-3 FPGA. In [3], Mohamed Ramdani *at al.* provide a non-exhaustive review of the research work conducted in the field of electromagnetic compatibility (EMC) at the IC level over the past 40 years with focus on measurement methods and modeling approaches. In [4], Jan Mocha *et al.* presented an approach that compared the conducted and radiated EME generated by two processor systems implemented in a FPGA. The same program was used in both processor systems. However, one of the systems was build using only internal resources of the FPGA, while the other used external SRAM as the program memory. In [5], authors presented and discussed the results of testing EME generated by circuits implemented in Xilinx FPGAs XC 4025E and XCV 800 types. Both radiated and conducted emissions of the circuits were measured as a function of clock frequency. At the end of this work, authors presented possible practical recommendations to minimize EME level. In [6] and [7], authors developed a customized platform tailored for combined tests of total ionizing dose (TID) radiation and electromagnetic interference (EMI). This platform is dedicated to Xilinx Spartan and Virtex FPGAs. In the sequence, they validated the platform by analyzing the single-event upset (SEU) sensitivity of a SRAM-based FPGA to the combined effects of EMI and TID-imprinted values.

Nevertheless, from the best of our knowledge it is worth noting that none of the previous works found in the literature was dedicated to study the effect of logic place and route (P&R) on the EME level of FPGA. Dealing to minimize this gap, this paper analyzes the impact of the P&R process of logic inside the FPGA on the emission level of such component. Though, a softcore version of the processor Hellfire RISC [8,9] was placed and routed in three different ways in a commercial FPGA (Xilinx/Spartan 3E, part number XC3S500E-4PQ208). In order to measure EME of such embedded system, three experiments were performed. The first experiment measured the far-field emission from voltage raw measurements at GTEM cell terminal [10]. The second experiment was based on measuring the near magnetic field using a fixed H-field probe within a small anechoic chamber as shielded housing to minimize ambient noise. Then, the last experiment was based on the so-called Surface Scan Method [11]. This measurement technique enables the visualization of the near magnetic field directly at the surface of an IC package or microchip. In this case an H-field probe is automatically

moved step by step over the surface of the IC. At each position, the magnetic field is measured with the help of e.g. a spectrum analyzer in a certain frequency position or range.

The remainder of this work is organized as follows: Section II describes the performed experiments, proceedings and laboratory set-up. Section III presents the case-study based on the Hellfire RISC softcore processor, application code and P&R strategies for the FPGA. Then, Section IV discusses the obtained results and suggests further directions of the research. Finally, Section V draws the final conclusions of the work.

II. Performed Experiments

In order to observe the effect of the place and route (P&R) algorithm on the FPGA emission level, three experiments were performed as described in the sequence.

A. GTEM Cell Test Method

The first experiment, based on the GTEM Cell Test Method [10,14,15], was performed at the LAAS-CNRS and is depicted in Fig. 1. The FPGA board was placed within the GTEM cell in a fixed position. Its activity was controlled by a Test Host Computer (THC) placed outside the GTEM cell. The voltage induced at the GTEM cell terminal by the FPGA radiation was measured with a spectrum analyzer. If the FPGA board is assumed to be electrically small and equivalent to an elementary electric dipole, the far-field emission from the FPGA board can be estimated at any distance (in this experiment, at 1m) [12]. In spite of these assumptions, the results can be compared with typical radiated emission requirements at electronic equipment level.

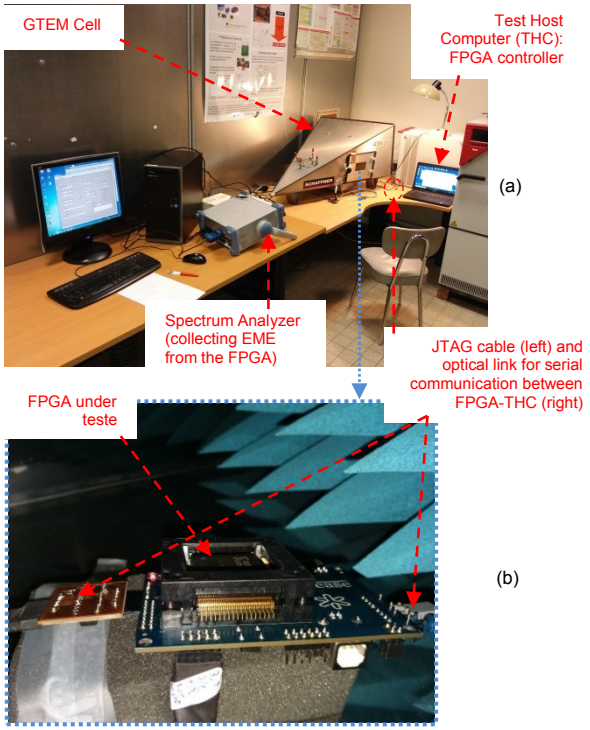


Fig. 1. GTEM Cell Test Method experiment set-up at LAAS-CNRS: (a) general overview; (b) detail of the FPGA under test.

The GTEM cell primarily estimates the far-field emission of the FPGA including the emission generated by the PCB on which the IC is mounted on. In contrast to that, the two near field measurement techniques (*Sections B* and *C* described hereafter) have been chosen to have a good comparison between far and near field of the generated emission by measuring only the silicon die contributions. For the experiment described in *Section B*, a big near field probe was located in a fixed center position on top of the IC package to measure the magnetic field contribution of the whole die. Unlike to this, in the last experiment (*Section C*) the focus was set to localize the near magnetic field distribution over the die surface by using a very small, moving near field probe, which offered a very high local resolution. These methods constitute effective methodologies to characterize integrated circuits in terms of EME.

B. Anechoic Chamber with Fixed Near-Field Probe

The second experiment, based on a near-H field probe located within a small anechoic chamber which was used as shielded housing to minimize ambient noise, was performed at the TU Graz University (see Fig. 2). The H-field probe was placed approximately 2mm above the surface of the ICs package. For all measurements the probe was at the same position. The output voltage of the near-field probe was measured using a spectrum analyzer.

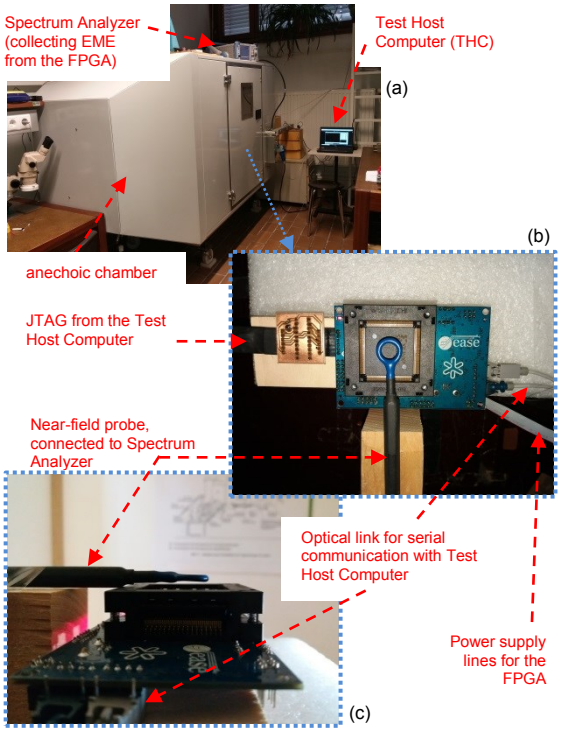


Fig. 2. Anechoic chamber with near-field probe experiment set-up at TU Graz: (a) general overview; (b) and (c) details of the FPGA under test.

C. Surface Scan Method with a Moving Near-Field Probe

The third experiment, based on the Surface Scan Method [11,13,16], was also performed at the TU Graz University (Fig. 3). This method constitutes an effective methodology to characterize printed circuit boards and integrated circuits in terms of electromagnetic emission (and immunity as well). It is a useful technique to locate areas of critical radiation or

susceptibility, which could influence the performance of devices nearby or the device under test itself. Fig. 3 depicts a photo of the test set-up. The equipment seen in this figure consists of a micromanipulation (wafer probing) that is equipped with stepper motors to control the probe movement in XYZ directions (in our experiment, Z was fixed to a constant value of 2mm). Note that while the aforementioned experiment measured emission based on a fixed probe position with respect to the FPGA package, this experiment scanned 4,000 points above the surface of the package with a moving near-field probe where the chip is located, hence adding a much higher precision and sensitivity to the emission measurement.

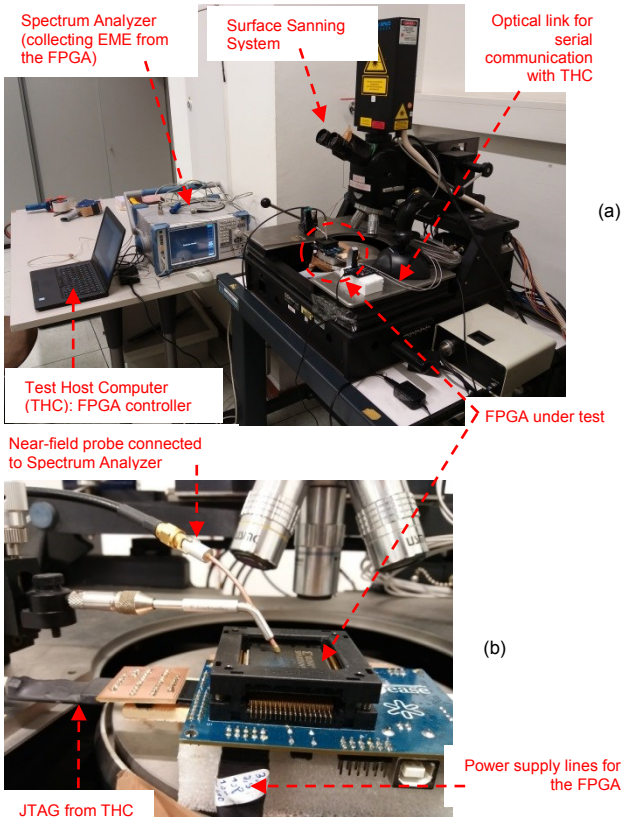


Fig. 3. Surface Scan Method experiment set-up at TU Graz: (a) general overview; (b) detail of the FPGA under test.

III. Case-Study: HW, SW and Place & Route Strategies

The case-study was based on a Spartan 3E FPGA (part number XC3S500E-4PQ208), from Xilinx, which was mounted on a dedicated board specially designed to support EMC test [6]. The board design and software development were carried out by the Catholic University – PUCRS. In order to analyze the effect of the P&R algorithm on the FPGA emission level, a softcore processor: Hellfire RISC running a Bubble-Sort program over an operating system (HF-OS) [8,9] was placed and routed in three different configurations in the Spartan 3E FPGA. In the first configuration, the processor was placed and routed automatically by the ISE-EDK Design Tool of Xilinx without designer assistance (let us say this is the "Automated" P&R version). In the second and third configurations, the processor was completely and intentionally sat in the periphery region ("Center" version) and in the left-hand side ("Right" version) of the configurable logic block (CLB) array of the FPGA. With this purpose, the designer prevented the ISE-EDK Tool from instantiating the processor core in the center of the CLB array (Center version) and in the right side of the CLB array (Right version), respectively. Fig. 4 depicts these three P&R strategies. See also Fig. 5, which depicts the embedded system basic block diagram.

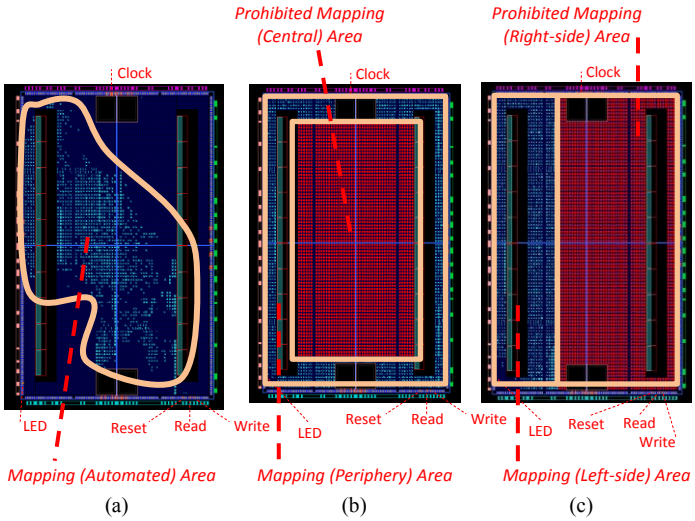


Fig. 4. Three P&R strategies to instantiate the processor core inside the CLB array of the FPGA: (a) "Automated", (b) "Center", (c) "Right".

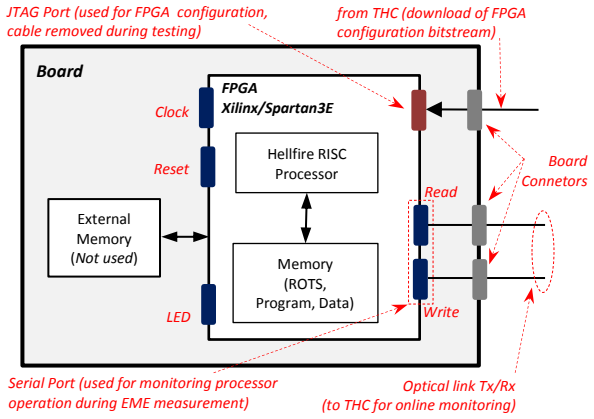


Fig. 5. Overview of the embedded system: FPGA and board.

In order to prevent board-level signals from jeopardizing FPGA EME measurements, the whole system (i.e., processor and memory containing operating system, program and data) was mapped inside the FPGA. The only signals flowing on and outside board during EM emission measurement were those associated to the serial communication connecting the FPGA to the user test host computer (THC). This serial port was used to monitor processor operation in real time during the experiments. In order to prevent communication from being disrupted by electromagnetic interference during the experiments, the serial communication was implemented by means of a two-module optic fiber link (Tx/Rx). Figs. 4 and 5 (five blue dots) depict the pin positions configured around the

FPGA CLB: "Read" and "Write" (for the serial communication), "LED" (to monitor FPGA operation), "Clock" and "Reset". The pin positions were fixed for all three P&R configurations. Additionally, a JTAG connection was used to configure the FPGA (Fig. 5, red dot). Once the configuration was complete, the cable was removed before starting EME measurements.

IV. Obtained Results

Fig. 6 summarizes the EME measurements. Fig. 6a depicts results for the LAAS-CNRS experiment, whereas Figs. 6b and 6c present results for the two TU Graz experiments. Table I summarizes the ambient noise values measured for the three experiments. The ambient noise was measured by disconnecting the board under test from power supply lines and then, the Spectrum Analyzer captured the remaining noise around the FPGA.

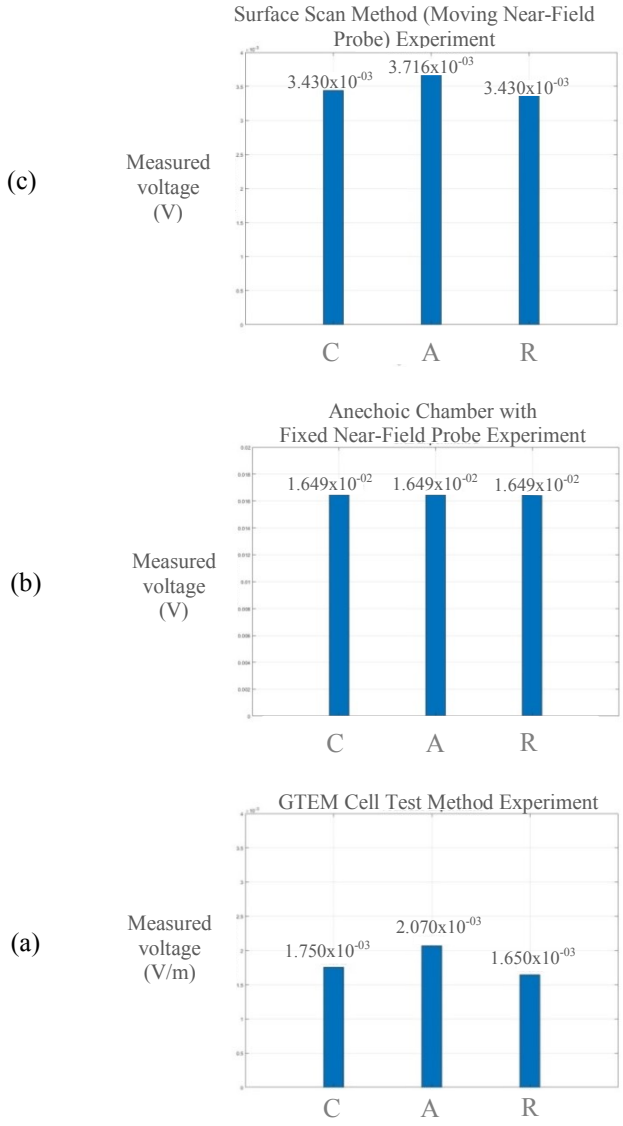


Fig. 6. EME measurements for the three FPGA P&R strategies (C: "Center", A: "Automated", R: "Right"), performed during the three experiments: (a) GTEM Cell Test Method; (b) Anechoic Chamber with Fixed Near-Field Probe; (c) Surface Scan Method (Moving Near-Field Probe).

By observing Fig. 6 and Table I, the following conclusions can be taken:

a) In Fig. 6a, the emission level of the "Automated" place and route version is 21.8% higher than the average of the other two configurations ("Centered" and "Right" versions). Note that the GTEM Cell Test Method measures EM emission from the whole system, i.e., not only from the FPGA but also from the board (including tracks and other components such the serial/optical converter logic sitting around the FPGA).

TABLE I. AMBIENT NOISE MEASURED FOR THE THREE EXPERIMENTS

Experiment	Ambient Noise
Surface Scan (Moving Near-Field Probe) Method	3.297 x 10-3 (V)
Anechoic Chamber with Fixed Near-Field Probe	4.766 x 10-3 (V)
GTEM Cell Test Method	8.938 x 10-4 (V/m)

b) In Fig. 6b, the emission level of the three P&R strategies is similar: 1.649 $x10^{-2}$ volts. This experiment was not able to identify different emission levels among the threes strategies, as did the other two experiments of Fig. 6a and 6c. This could be explained by the fact that the measurements in the small anechoic chamber were performed under 44.56% higher ambient noise than the other near-field technique ($4.766x10^{-3}$ volts against $3.297x10^{-3}$ volts, Table I). This high noise level may have jeopardized the results in such a way that EME measured from the FPGA was observed to be in the same order of magnitude for the three P&R strategies.

c) In Fig. 6c, the EM emission level of the "Automated" place and route version is 8.4% higher than the other two configurations ("Centered" and "Right" versions).

V. Conclusions

This work presented a preliminary study about the impact of the place and route (P&R) strategy on the electromagnetic (EM) emission level of a commercial FPGA. The considered device was a Xilinx Spartan 3E, part number XC3S500E-4PQ208, which was configured with the Hellfire softcore RISC processor available in the *github* public domain. The FPGA was mapped by three different strategies: "Automated", in which the processor was placed and routed automatically by the ISE-EDK Design Tool of Xilinx. In the second and third versions, the processor was completely and intentionally placed in the left-hand side ("Right" strategy), and in the periphery region ("Center" strategy) of the configurable logic block (CLB) array of the FPGA. The processor executed a Bubble-Sort program running over an operating system (OS).

The obtained results suggest that the P&R strategy can affect the FPGA emission level. For the developed experiments, the influence was in the order of 21.8% (GTEM Cell Test Method) and 8.4% (Surface Scan Method). The anechoic chamber with fixed near-field probe experiment presented high ambient noise at laboratory, which prevented us from getting measurements with sensitiveness high enough

to discriminate the emission levels generated by the three P&R strategies.

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