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Feasibility of Standalone TDoA-based Localization Using LoRaWAN

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***Abstract*—The growing need for localization has created an array of alternative approaches to GNSS, based on Wi-Fi, Bluetooth, Ultra-Wideband, etc. Long Range Wide Area Network (LoRaWAN) is one such technology that has garnered tremendous attention due to its low power and long-range capabilities. Many attempts to achieve localization using LoRaWAN have been made till now, based on a variety of techniques such as Angle of Arrival (AoA), Time Difference of Arrival (TDoA), Received Signal Strength Index (RSSI). In this paper, we present a novel, standalone localization approach by developing a collaborative, TDoA-based methodology using LoRaWAN. The server determines the target node location by means of TDoA measurements from the target node to the gateways. The introduction of an additional stationary node allows the synchronization of the gateways without utilizing GNSS, either inbuilt or external. The cooperation between target node, synchronization node and server, is the innovative feature which makes this approach attractive for GNSS-free localization. Further, we explore the effects of timing resolution, time-on-air, and duty cycle constraints on the localization error. Finally, the distribution of error in a triangle of gateways situated approximately 8.6 kilometers apart is simulated in ideal Line of Sight (LoS) conditions, showing the maximum error to be around 23 meters.**

***Index Terms*—IoT, Localization, LoRaWAN, TDoA, GNSS-free.**

I. Introduction

Global Navigation Satellite System (GNSS) is the leading technology for localization and real time tracking of a subject [1], foremost advantages being the wide coverage and availability in open space environments, high accuracy and the ease of integration into many applications. The major disadvantages are: (i) high power consumption of standalone GNSS receivers; (ii) limited coverage and accuracy in harsh environments characterized by either the absence of direct line of sight (LoS) between the receiver and the satellite or a massive multipath phenomenon, such as urban and indoor environments [2]. A possible solution to cope with these limitations is to reasonably integrate low-cost hardware sensors to GNSS solutions. However, there are significant trade-offs, including increased costs, complexity of localization algorithms and power consumption. This has resulted in a shift towards alternative technologies including cellular networks (GSM, OFDM-based) [3], Wi-Fi [4] and Ultra-Wideband (UWB) [5]. Further, the surge in the number of low power devices, largely due to the development of Internet of Things (IoT) technologies, has resulted in a rise of GNSS-free alternatives for localization using Low Power Wide Area Networks (LPWANs).

Among these networks, Long Range Wide Area Networks (LoRaWANs) [6] convey sensor information using very low power *end devices* to all *gateways* (i.e., base stations) in their transmission vicinity through Long Range (LoRa) wireless communications [7]. The gateways then relay all received replicas to a *network server* over a reliable back-hauling network. Any frame received at a gateway is forwarded together with the measured RSSI and time of arrival values [8]. Herein, the idea of using LoRaWAN for radio localization [9] definitely seems reasonable for the inherent possibility of adopting signal multi-lateration. Indeed, a plethora of approaches based on TDoA, RSSI, AoA, etc. have emerged. The key advantages of LoRaWAN over traditional approaches such as Wi-Fi and GSM-based methods, are high resilience to multi-path fading over long distances [10], [11], and the ability to choose power consumption to be low or high, in line with the specific use cases [12]. This goal is achieved through a proprietary modulation owned by Semtech [13], that relies on the Chirp Spread Spectrum (CSS) technique [14]. However, LoRaWAN is relatively new, which leads to low adoption rate and availability of infrastructure, especially outside of USA and Europe. Nevertheless, the advantages far outweigh these disadvantages, particularly with more and more countries jumping on the LoRa bandwagon. The fact that localization has become an even more integral problem in a variety of research areas including robotics [15], Wireless Sensor Networks (WSNs) [16], indoor tracking and positioning [17], and autonomous driving [18] encourages further research on this problem.

Remarkably, to the best of our knowledge all previous TDoA-based approaches for LoRaWAN still rely on GNSS systems for synchronizing time on gateways. In these cases, gateway synchronization is attained by passing the source timing information taken from GNSS (through any other technology) to the destination LoRa transceiver. This is true for certain GNSS-free deployments as well [19], where it had been used as a one-time synchronization aid. Such an approach requires sophisticated circuitry that is able to cancel out timing misalignment between source and destination clocks, which comes at an increased cost. In this paper, the cooperation between end devices, gateways and network server is exploited to obtain a standalone localization approach, relying only on LoRaWAN. This methodology becomes potentially attractive for GNSS-denied localization applications and is ideally meant to work with low-cost gateways. We present an innovative networked approach to achieve gateway synchronization without GNSS, entailing an additional node in the network reserved for synchronizing the gateways. Transmissions from this node are then exploited by the gateways to simultaneously reset their timing references, resulting in synchronized ToA values. As detailed in section III, this approach also necessitates an additional synchronous counter and when a 25 MHz clock is used, the maximum error obtained is 23 meters. Indeed, transmissions from this additional synchronization node can easily consume a significant portion of bandwidth in an already very low-throughput network (the default LoRaWAN access scheme is pure ALOHA based). However, the mitigation of bandwidth waste due to localization overhead and collisions will be tackled in future works. In this paper, we assess the feasibility of the proposed localization system as long as it is able to provide a target precision in the position estimation. To accomplish this goal, we have dealt with realistic LoRaWAN settings by incorporating duty cycle limitations into our simulations [20]. The rest of the paper is organized as follows. Section II outlines the relevant related works on various localization techniques. Section III discusses the core idea of the paper, presents the error analysis and the corresponding design problem. Section IV elaborates the simulation methodology and results. Finally, section V draws conclusions and future scope.

II. Related Work

As stated already, alternative localization technologies to GNSS have been on a steady rise. However, they are mainly plagued by poor synchronization capability between the receiver modules and the low precision of the oscillators used as timing references. Usually, these issues are tackled by the use of external modules such as GNSS timing references, or by using algorithms to achieve asynchronous localization [21]. In general, WSN-based cooperative localization is the most developed alternative to GNSS [22], using both time-based [23] and RSS-based [24] methods.

More recently, protocols such as LoRa and Sigfox emerged as potentially better alternatives, owing to much longer ranges and lower power consumption, with applications in both indoor and outdoor scenarios. In [19], geolocation using TDoA values obtained at LoRaWAN gateways and synchronization using GPS modules was achieved, with a reported accuracy of 100 meters in locating a static device. Kalman filtering for time-based LoRaWAN localization was explored in [25], with similar reported accuracies. In [26], fingerprinting was applied to LoRaWAN and Sigfox in diverse urban and rural scenarios and the compiled datasets were made open-source. Preliminary results indicated mean location error to vary between 214.58 meters and 398.40 meters respectively, for rural and urban datasets of LoRaWAN. Utilizing these same datasets, a mean error of 322.63 meters and a median error of 193.63 meters were achieved employing an ensemble learning-based outdoor positioning algorithm, in [27]. In [28], RSSI-based localization techniques were explored using four different protocols, i.e., Wi-Fi, Bluetooth Low Energy (BLE), Zigbee and LoRaWAN, comparing localization accuracy and power consumption. An experimental performance evaluation comparing externally synchronised TDoA-based and RSS-based positioning techniques in a realistic LoRa network was presented in [29], concluding that TDoA easily outperforms all investigated RSS approaches. Further studies, on a pre-processing algorithm for dropping outlier TDoA values [30] and combining AoA and TDoA measurements [31] demonstrated an improved localization accuracy. In particular, the latter demonstrated that the average error is 73% lower in comparison to the standard TDoA based approach.

III. The Proposed Idea

A. Theory

As already introduced, the principal issue with time-based techniques is the lack of synchronization between gateways and till now this has been solved by using GNSS receivers, either inbuilt or external. To make our solution truly GNSS-free, we place a stationary synchronization node at a known location (x_0, y_0) in the area covered by the gateways, whose sole task is to assure this synchronization. For example, it can be temporally "equidistant" from the gateways, i.e., a signal sent from that location will reach all gateways at the exact same time, after adjusting for the presence of real-world obstacles. This signal is a special message that specifies each gateway to reset a synchronous n-bit counter that is used to obtain the time of arrival values. The counters on all the gateways are reset simultaneously upon receiving this signal, providing synchronized time of arrival values between consecutive resets. The n-bit counter keeps time to a precision of the order 10^{-9} seconds.

The reason for an additional counter is that the Real Time Clock (RTC) inside each gateway is not accurate enough for localization. These RTCs are also responsible for time-stamping various events including downlink and uplink transmissions, error messages, etc. which do not require high precision. Thus, they are synchronized with the outside world less frequently. However, high precision is a stringent requirement for localization; for instance, if we assume a 5 parts per million (ppm) drift in the RTC, the clock drift error

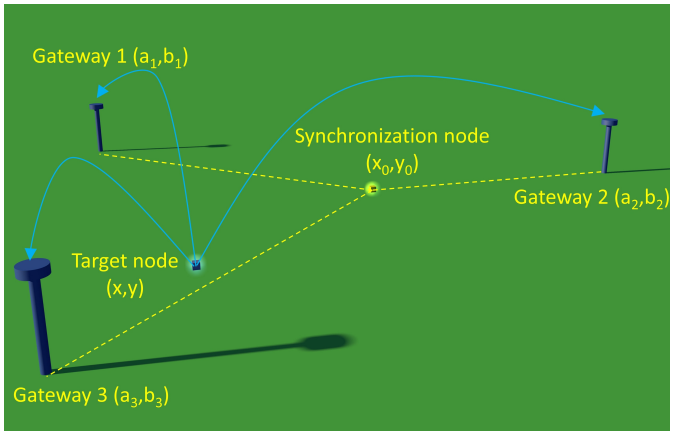


Fig. 1. A schematic representation of the proposed system. The synchronization node is placed at a known location (x_0, y_0).

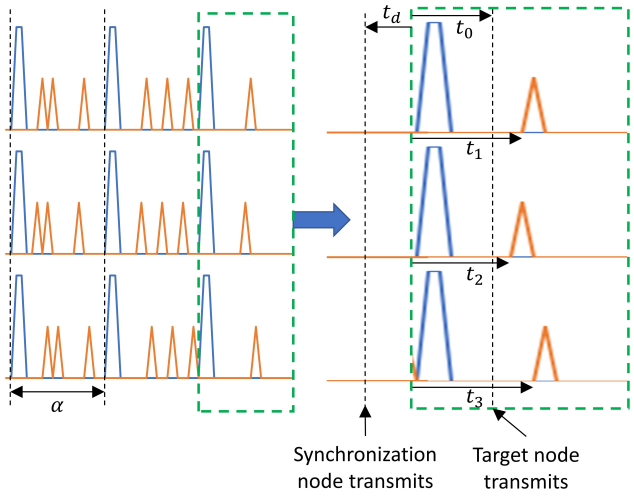


Fig. 2. An illustration of the signals received at each gateway. The blue signals are transmissions from the synchronization node, while orange represents transmissions from the target device.

alone accumulates to 10^{-3} seconds every 200 seconds. This is completely unusable for localization as this translates to an error of the order of 10^5 meters. To mitigate this, the synchronization with the network server needs to happen every 10^{-2} seconds to keep the error in the 10^{-9} second range (or equivalently, in the meter range). This high frequency of transmissions between the gateway and server affect the aforementioned tasks of the gateway and can also increase its power consumption significantly. Thus, a simple n-bit counter is employed, keeping time as multiples of a predetermined value. The effect of resolution of the counter (value of n) on error is detailed in further sections. A noteworthy point here is the requirement of just three gateways for calculating the unknowns. It is also worth mentioning that this problem has been considered in 2D because this is the most typical scenario envisaged in the targeted applications for LoRaWAN localization. This translates to a huge reduction in the setup cost, even after considering the cost of the additional synchronization node.

The location estimation of the target node after the synchronization of gateways is a fairly well-researched problem. As seen in Fig. 1, the coordinates of the three gateways are (a_i, b_i) and the time of arrival values of the signal sent from the target node at (x, y) as captured by the synchronized counter at each gateway are t_i, where i takes integer values 1, 2 and 3. Line-of-Sight (LoS) conditions are assumed and the impact of noise on the accuracy of the estimation of t_i has not been considered in this contribution. Equating the distance between the target node and gateways to the product of speed of the signal and time of travel gives

$$\sqrt{(x-a_i)^2+(y-b_i)^2} = c(t_i - t_0) = d_i \tag{1}$$

where t_0 is the time at which the target node initiates transmission. The propagation speed of the signal is given by c, the speed of light. This non linear system of equations has three unknowns, x, y and t_0. This is usually solved by eliminating t_0 and applying multilateration algorithms on the resulting two equations (TDoA method). One such solution is detailed in [32], as

$$x = \frac{(b_2-b_1)\gamma_1 + (b_2-b_3)\gamma_2}{2[(a_2-a_3)(b_2-b_1)+(a_1-a_2)(b_2-b_3)]} \tag{2}$$

$$y = \frac{(a_2-a_1)\gamma_1 + (a_2-a_3)\gamma_2}{2[(a_2-a_1)(b_2-b_3)+(a_2-a_3)(b_1-b_2)]} \tag{3}$$

where

$$\gamma_1 = a_2^2 - a_3^2 + b_2^2 - b_3^2 + d_3^2 - d_2^2 \tag{4}$$

$$\gamma_2 = a_1^2 - a_2^2 + b_1^2 - b_2^2 + d_2^2 - d_1^2 \tag{5}$$

B. Error Analysis

The sources of error are the measured quantities, t_i (or d_i, equivalently) from equation (1). The localization error is taken as the distance between the actual location of target node and the calculated location. To model the errors in t_i, it is imperative to inspect the path of the signal (flow of packets) as shown below.

The synchronization node transmits special packets every α seconds, denoted by the blue pulses in Fig. 2, which is a simplistic representation of the dataflow focusing on the signal path, ignoring channels and bands. Building on our assumption of temporal equidistance, Fig. 2 depicts the blue pulses to be arriving at the same instant t_d at all gateways, i.e., the instant of frame arrival at the i-th gateway is $t_{d_i} = t_d$. However, this is not compulsory. The values of t_{d_i} can be different for each gateway and still aid in synchronization, as they can always be calculated from the *known* position of the synchronization node. This perpetual knowledge of the synchronization node's position is the only requisite. The choice of α depends on the resolution of the counter used, which itself depends on a slew of factors including power consumption, design complications, and the cost of the setup. The orange triangular pulses in Fig. 2 denote the packets sent from the target node. For the t_i

values to be accurate, orange pulses/target node transmissions should only occur between consecutive synchronization node transmissions/blue pulses. Also, the resetting behavior of the counter means that t_i is non-negative for any gateway. t_0 is also non-negative because it is always measured with respect to the previous synchronizing signal, and t_{d_i} is always negative as the transmission from the synchronization node always happens before the synchronization.

The possible sources of error in the above outlined data path are: (i) Error in the position of synchronization node; (ii) Oscillator drift in the crystals of both the additional counter and inbuilt processor of the gateway; (iii) Least count of the counter (rounding off error) and (iv) Clock slippages in the gateway processor during various operations. For instance, there will be a delay between receiving the synchronization packet and the counter resetting. A similar analogy can be drawn to other transmissions and operations, including calculating the time of arrival values. There will be a delay between receiving the target node packet and the counter registering the time of arrival value. This delay can be significant in this scenario because time is being counted in the order of 10^{-9} seconds. Modelling the error in t_i with these variables,

$$e_{t_i} = \Delta t_{d_i} + N_i\omega_{1i} + \mathcal{U}_{2i}\left[0,T\right] + \mathcal{U}_{1i}\left[0,k_i\right]\cdot\left(T_g + \omega_{2i}\right) \quad (6)$$

where i represents the i^{th} gateway. The Gaussian distributions $\omega_{1i} \sim \mathcal{N}(0,\sigma_{1i}^2)$ and $\omega_{2i} \sim \mathcal{N}(0,\sigma_{2i}^2)$ with zero mean and adjusted variances model the drift in the counter and processor clock, whose time periods are denoted by T (frequency = f) and T_g (frequency = f_g) respectively. N_i is the multiple of T stored in the counter corresponding to the t_i value, that varies between 0 and 2^n. $\mathcal{U}_{1i}$ is a discrete uniform distribution to model processor clock slippages (k_i being the maximum number of clock slippages) and $\mathcal{U}_{2i}$ is a uniform distribution to model the rounding off error in the n-bit counter. Δt_{d_i} denotes the offset due to the error in position of the synchronization node, given by

$$\Delta t_{d_i} = \frac{(x_0 - a_i)\Delta x_0 + (y_0 - b_i)\Delta y_0}{c^2 t_{d_i}} \quad (7)$$

Equation (6) is the comprehensive model of total error possible in this scenario whereas in reality, there might not be two different crystal oscillators for the processor and the n-bit counter. For instance, the clock of the counter can be generated from the main processor clock using frequency multipliers. To determine the critical design parameters of this system, it is important to consider the relative contributions of these components in the total error. In equation (7), the distance between the synchronization node and the i^{th} gateway is given by ct_{d_i}, which is of the order of 10^3 to 10^4 meters. The difference in coordinates in the numerator is also of the same order. Errors in synchronization node coordinates denoted by Δx_0 and Δy_0 respectively, are ideally in the 10^{-2} to 10^{-1} meter range, which implies that Δt_{d_i} is in the range of 10^{-9} to 10^{-10} seconds.

If we assume the processor frequency to be 400 MHz (T_g = 2.5 ns) which is the same as the ARM9 Processor found in the MultiConnect® Conduit™ (Model Number : MTCDT-246A-US-EU-GB), an exaggerated 100 clock slippages will still result in an error of the order of 10^{-7} seconds. Similarly, if the counter clock frequency is assumed to vary between 10 MHz and 200 MHz, the rounding-off error is of the order of 10^{-7} seconds. As stated already in III-A, clock drift error can be in the range of 10^{-3} to 10^{-2} seconds, which implies it is indeed the major contributor. However, clock drift is an extensively researched problem at the same time. Compensation techniques range from the use of differential TDoA (DTDoA) [33] and novel time synchronization schemes [34], [35] as after-the-fact solutions to using techniques including temperature compensation while designing the oscillator itself [36], [37]. Also, none of the experimental results detailed in Section II discuss clock drift errors, further reinforcing our assumption that they can be predicted and cancelled out. Hence, we assume that drift is negligible and discard it from our model in equation (6).

Another important constraint to consider in our pursuit of optimizing for least error is the duty cycle (δ), which is restricted for LoRaWAN in some geographies. For example, it is restricted to be less than 10% in Europe (India has no restrictions as of now). Thus, we need to conduct this error analysis from a design problem perspective.

C. The Design Problem

The goal of modelling errors and running simulations is to optimize for the least error in localization, while staying within the duty cycle limitations. Hence, maximum acceptable mean error in localization (e_{max}) and maximum duty cycle allowed (δ_{max}) are our primary design constraints. For this section, we assume the clock slippages and drift to be negligible, thus, equation (6) becomes

$$e_{t_{ideal}} = \mathcal{U}_2\left[0,T\right] \quad (8)$$

or

$$e_{t_{ideal,max}} = T \quad (9)$$

Duty cycle is the ratio of the time-on-air (τ) to the total time period between successive transmissions (2^nT). This ratio should always be less than the maximum allowed duty cycle. Thus,

$$\delta = \frac{\tau}{2^n T} \leqslant \delta_{max} \quad (10)$$

which implies that the primary design variables are τ, T (or f) and n. T is determined by e_{max}, which is then used to choose the appropriate values of τ and n to satisfy the constraint of δ_{max}. However, e_{max} can be simulated only when the orientation of gateways is known. This depends on the range of LoRa in the deployment terrain, which depends on the Spreading Factor (SF) used [10]. Time-on-air is also dictated by the SF used, among other factors including symbol duration, bandwidth, data rate, etc. [38]. Hence, SF acts as a secondary design constraint, limiting the range of τ before duty cycle constraints and affecting the values of T indirectly. Another secondary design constraint is T_g, limiting the precision to choose T. As stated already, the additional

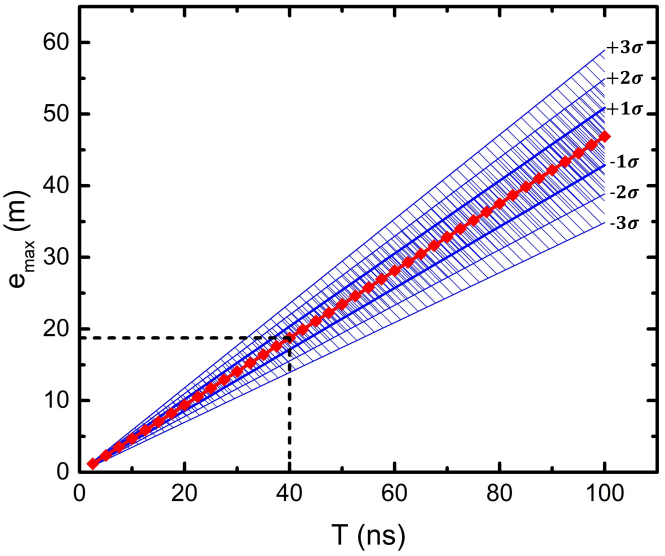


Fig. 3. Variation of e_{max} with T. e_{max} is the maximum acceptable mean error at any position within the triangle and T is the time period of the n-bit counter clock. The shaded regions indicate the confidence intervals of 1, 2 and 3 sigma.

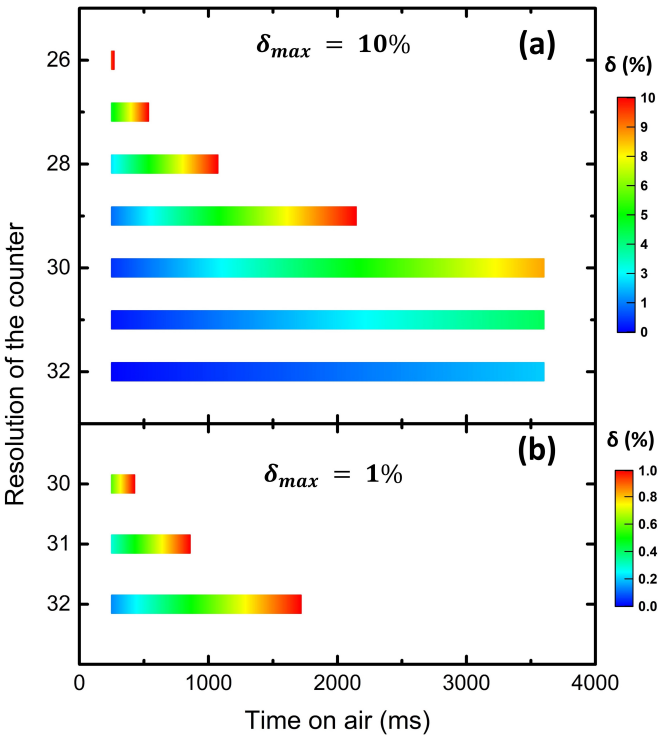


Fig. 4. Variation of duty cycle δ with the time-on-air (τ) and the resolution of the counter (n). (a) δ limited to 10%. (b) δ limited to 1%. The value of T is taken as 40 ns.

clock for the n-bit counter is likely to be generated from the processor clock, hence a faster processor clock or lower T_g gives us higher precision to choose T. Lower T_g also reduces error due to clock slippages as seen from equation (6).

In the set of values of T allowed by e_{max}, the maximum value should be chosen to minimize the duty cycle. In the case of n, a lower bit resolution drastically reduces the effect of oscillator drift, but increases duty cycle exponentially at the same time. Hence, it needs to be tuned accordingly. Similarly, τ also needs to be tuned to minimize duty cycle by varying spreading factor (if the LoRa coverage allows multiple spreading factors in that particular deployment), coding rate, etc.. T and n are further constrained by the overflow of the counter; faster clock and low n result in a quicker overflow, while slower clock reduces the precision of the measured time. Hence, the values for the variables τ, T and n have constraints and both upper and lower bounds, requiring the system design to be a trade-off between these depending on the deployment environment.

IV. Simulations

To simulate for the maximum error possible with our assumptions, the gateways are positioned at the vertices of an equilateral triangle circumscribed by a circle of diameter 10 km and centered at the origin, effectively resulting in a maximum transmission distance to be around 8.6 km (the side of the triangle). This coverage is achievable only by using the highest spreading factor, SF12. While higher ranges upto 15 km are possible on ground deployments as evaluated in [39], the same study also calculated packet losses to be as high as 74% beyond 10 km. This can prove to be costly in the context of localization, especially in the case of synchronization packets in our architecture. The vertices of the triangle are at $(0, -5000)$, $(4330.13, 2500)$, and $(-4330.13, 2500)$. Since any area of deployment is regularly tessellated by equilateral triangles, the analysis performed on this single triangle can be extended to the entire area. The location of the target node is generated randomly inside this triangle, and the corresponding TDoA values are calculated from equation (1). The processor clock is assumed to be 400 MHz (T_g = 2.5 ns).

The first simulation establishes the relation between e_{max} and T. For the calculation of e_{max}, 106 points are taken at random inside the triangle. $e_{t_{ideal}}$ is taken to be its maximum value as given in equation (9) and to further assure that the maximum possible value of e_{max} is calculated, the 8 permutations that arise due to the sign of $e_{t_{ideal}}$ when added to the TDoA values corresponding to each of the 106 locations, are also considered. Thus, each of the 106 locations has 8 erroneous estimates calculated from the 8 erroneous sets of TDoA values as shown in equations (2) to (5). The maximum among those values is taken as localization error for that point. The mean of all the 106 values is taken to be e_{max}. The value of T is varied between 2.5 ns and 100 ns in steps of 2.5 ns and for each value of T, the same 106 points are considered and e_{max} is subsequently calculated. The results are shown in Fig. 3.

As stated already, the value of e_{max} limits T. Essentially, this translates to an upper bound on the time period of the counter clock T, denoted by T_{max} or a lower bound on its frequency f, denoted by f_{min}. The actual value to be taken

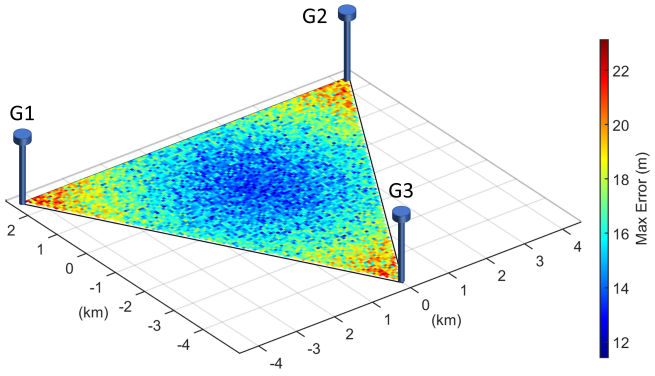


Fig. 5. Distribution of maximum localization error within the triangle for $T = 40$ ns, and $n = 32$.

is then determined by other considerations, duty cycle being the foremost among them.

The next simulation aims to reveal the restrictions because of the duty cycle constraint. By making T constant in equation (10), the choices of τ and n are explored. Since we are using only SF12, the values of τ are restricted between $0.25 - 3.60$ seconds. These bounds have been calculated with the aid of open-source air-time calculators available online, considering all possible bandwidths (125, 250 and 500 kHz), load packet lengths (51 bytes or lower for 125 kHz, 33 bytes or lower for 500 kHz) and coding rates $(0.5 - 0.8)$. We assumed T = 40 ns ($f = 25$ MHz). This choice assures a reasonably good precision while also keeping e_{max} at 18.75 m (Fig. 3). For a 32-bit counter, this also translates to an overflow time of 171.79 s, which is again a good balance.

A key point to note here is the lack of flexibility to choose n, even for a duty cycle as high as 10% as seen in Fig. 4a. While lower values of n like 4-bit and 6-bit counters for instance, drastically reduce drift as seen in equation (6), it has an equally catastrophic effect on the duty cycle because of the need for repeated transmissions. However, in the presence of drift compensation, it is reasonable to choose a 32-bit counter to reduce the duty cycle of the synchronization node. Lower resolutions, such as a 28-bit counter for instance, are viable options only when duty cycle is not very important and there are significant gains in other parameters including clock drift, low power consumption, simpler design, etc. It should be noted that the duty cycle variation in Fig. 4 is only for a predetermined constant value of T stated above and a slower clock can also be considered if duty cycle is of higher importance.

Finally, the variation of localization error within the triangle of gateways is calculated based on the values of the design parameters as $T = 40$ ns and $n = 32$ to serve as a basis for future studies. 7050 points inside the triangle are taken as the locations of the target node with e_t for each corresponding set of TDoA values given by equation (8). 23 values of e_t are taken at each location to indicate 23 transmissions from each position of the target node, each time with a different error in the values of t_i to mimic a real-world scenario. The same 8 permutations considered in Fig. 3 are also considered, and the maximum value of localization error among those 8 permutations and 23 transmissions is taken as the error at that location. The distribution of this localization error is as shown in Fig. 5.

The maximum error obtained in this simulation is approximately 23 meters. This is higher than the estimated 18.75 meters from Fig. 3 because that is an estimate of mean. The distribution in Fig. 5 shows higher error is likely close to the gateways (and away from the synchronization node), compared to the center of the triangle. This is intuitive because all the time of arrival values are relatively large leading to less effect of errors, compared with values from the edge of the triangle, where one of the values is very low.

V. Conclusion and Future Scope

In this paper, a novel and standalone TDoA-based localization approach using LoRaWAN was proposed. The problem of asynchronization between the gateways was solved by a GNSS-free, collaborative methodology entailing a stationary synchronization node. An error analysis for the approach has also been presented detailing the effects of many factors including drift, clock slippages and clock frequencies on the localization error. The consequences of duty cycle restrictions were also studied, modelling the analysis as a design problem with localization error and duty cycle limitation as design constraints. Finally, simulations exploring the relation between design variables including resolution and clock frequency of counter and time-on-air with the design constraints were also carried out. The distribution of localization error at different locations inside the triangle of gateways was also simulated.

The extent of future work in this area is vast, as this paper largely deals with proposing the initial idea and theoretical considerations for the setup. The reason for such a distribution with low errors in the central region of the triangle and the effect of adding clock drift and slippages are some of the interesting insights that can be explored in more detail. Furthermore, the impact of both synchronization signal overhead and frame collisions on the bandwidth usage will be carefully investigated in order to bound the range of applications benefiting from such an approach. Remarkably, the synchronizing function of the synchronization signals can also be performed by frames sent from LoRa-enabled smartphones carrying GNSS information. This possibility introduces an architectural simplification (synchronization node not required) but raises a wide spectrum of research challenges mainly due to the unpredictable position of the synchronizing devices and the consequent impact on network performances. We are also currently working on extensive experimental verification and performance evaluation of this architecture.

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