Design Method for Reconfigurable Low Noise or Highly linear LNA

Bastien Pinault, Jean-Guy Tartarin, R Leblanc, A Jourier

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B. Pinault[1,2], J.-G. Tartarin[1,2], R. Leblanc[3], A. Jourier[3]

[1] *LAAS-CNRS, 7 Av. du Colonel Roche, 31400 Toulouse*
[2]*Université Toulouse III - Paul Sabatier, 118 Rte de Narbonne, 31062 Toulouse*
[3] *OMMIC SAS, 2 Rue du Moulin, 94450 Limeil-Brévannes, France*
bpinault@laas.fr, tartarin@laas.fr

***Abstract*—In this article we introduce a new method for designing robust low noise amplifier (LNA) using wide bandgap GaN MMIC technology. The objective of this work is to compare different design strategies, which manages the combination of optimum noise figure with high linearity. This article compares two conventional design strategies to design GaN LNAs, as proposed in the literature, with a new one allowing the reconfigurability of the LNA. If the classical methods are based on the selection of the active device for a targeted noise figure and its associated compression point, this work proposes an alternative design option that allows to change the noise figure and the linearity performances by applying dedicated DC biasing conditions to the transistor. Then, a comparison is performed for three different LNA design strategies, that are presented and discussed. It is demonstrated that the proposed reconfigurable LNA achieves the best NF results under nominal biasing conditions, while it can be tuned (by changing its biasing DC voltage) to improve its linearity and to avoid the loss of the signal under possible electromagnetic aggression. The new proposed LNA is simulated with noise figure better than 0.8 dB for a small signal gain higher than 9.5 dB over the 8-11 GHz frequency band, and with an input compression point (P1dB) as high as 21.3 dBm.**

***Keywords*—Low-noise amplifier, LNA, Gallium Nitride, HEMTs, Linearity, Circuit Topology, Reconfigurable, MMICs.**

I. INTRODUCTION

GaN HEMT offers higher linear performance and robustness than its GaAs or SiGe counterparts. Designers can take advantage of this specificity in robust low noise reception systems developed for modern applications such as military radar, altimetry detection or space communications front ends requiring systems capable of operating at high RF input. To satisfy this constraint without using any limiter before the LNA, one strategy is to oversize the transistor (larger physical and/or electrical dimensions than for optimum low noise conditions). Then non-linear performance is improved at the expense of the noise parameters [1]. This paper presents a comparative study on three different strategies for the design of GaN LNAs. Only simulations on single stage designs are presented for a fair comparison between each of these options, even if multi-stage LNAs have been designed. The considered frequency band is 8-11 GHz, and two LNAs are designed respectively for an optimum noise performance ($LNA_{\#1}$) and for an improved by 9dB IP_{1dB} ($LNA_{\#2}$): this compression point is selected to present a fair comparison with our reconfigurable version of $LNA_{\#tuned}$. Then we propose a third new strategy (based on $LNA_{\#1}$) to design an LNA that is able to be set both at its optimum noise performance condition but poor linearity, or that can be tuned to higher IP_{1dB} at the expense of degraded noise figure only by changing its DC quiescent point ($LNA_{\#tuned}$). The first section presents the technology which design kit is used for this study, and the sizing/biasing paradigm of the active device is presented. Then, the second section proposes the design of two conventional LNAs, i.e. the first one optimized only considering the noise or dynamic electrical performance (P_{1dB} is just simulated at the end of the design process), and the second one also taking account for the linearity (at the input of the LNA where the RF jamming must be considered). The third section focuses on our design strategy. The simulated noise and N.L electrical performances of the three LNAs are compared.

II. GAN TECHNOLOGY

The GaN technology selected for this comparative study on LNAs is the OMMIC D01GH process on silicon substrate. It provides HEMT devices with a transition frequency of 110 GHz, high breakdown voltage of 36 V, and a good power density of 4 W/mm. This process is suitable for RF High Power Amplifier (HPA), robust LNA and Transceiver modules.

In a conventional LNA design, the optimization of the first stage is performed on the four noise parameters (minimum noise figure NF_{min}, equivalent noise resistance R_n and complex optimum noise reflexion coefficient Γ_{opt}) and on the small signal parameters [S] criteria to respect the technical specifications imposed by the FRIIS formula in the reception system under study. The transistor sizing (number of gate fingers and gate length for a High Electron Mobility Transistors, HEMT) and its static biasing (V_{GS}; V_{DS}) are then selected

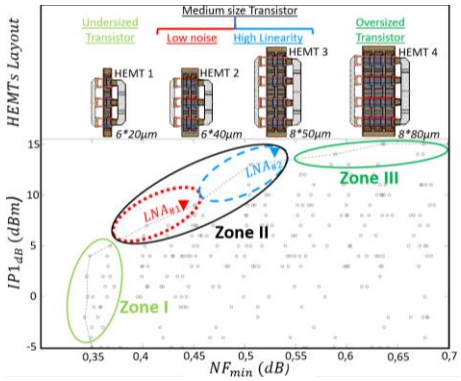

Figure 1 : Device biasing and sizing selection for Low Noise or high compression IP1dB purposes (NFmin versus IP1dB @10 GHz). Sizing is for number of gate fingers and gate individual width respectively ranging between [2;4;6;8] and [20 µm to 100 µm by step of 20 µm], while biasing on V_{GS} and V_{DS} respectively range between [-1,7 V to 0 V by step of 0.2 V] and [3V;5V;8V;12V;20V]

according to these aspects. Linearity of the receiver is then imposed by this selection. In Figure 1, the input compression point IP_{1dB} is plotted versus the minimum noise figure NF_{min} at the center frequency of 10 GHz. This mapping of the HEMT is developed for various sizing (number of gate fingers, gate individual length) and different biasing (V_{GS} and V_{DS}). The objective is to appreciate the possibility to get simultaneously low NF_{min} and high IP_{1dB} (even if these two parameters are not the only one to be considered for the design of an LNA). Four different transistors are reported in Figure 1 (one small, two medium and one large size devices) to illustrate the main trade-offs to operate for selecting the HEMT providing the appropriate value pairs (NF_{min}, IP_{1dB}). Of course, second order criteria such as the small signal gain, the noise or small-signal reflection coefficient magnitudes, the equivalent noise resistor are used to refine the active device selection. Three main areas are evidenced.

-The area labelled as zone I is not considered for this study, as the sizing and biasing of the transistor also increases the space between Γ_{opt} and S_{11}*, and that can be sensed through an increase of ΔNF (defined as $\Delta NF=NF_{50\Omega}-NF_{min}$). The effort to design the input matching network (IMN) degrades its losses, and as a consequence the final $NF_{50\Omega}$ of the LNA.

-Zone II is related to transistors exhibiting a low NF_{min}, and a high IP_{1dB} near the inflection between the low-noise and high- linearity sections in Figure 1. The lower trend (red dotted section) represents the most interesting features for the strategy of $LNA_{\#1}$ (best final $NF_{50\Omega}$) while the upper trend (blue dashed section) is more suitable for obtaining a highly linear $LNA_{\#2}$ (improved IP_{1dB}). It will be demonstrated that a good initial selection of the HEMT sizing will allow both NF_{min} and IP_{1dB} to be tuned by adjusting only the DC quiescent point for the design of $LNA_{\#tuned}$ (based on $LNA_{\#1}$).

-In zone III, the increase on NF_{min} for a poor benefit on IP_{1dB} will prevent the selection of these HEMT biasing and sizing solutions for the design of an LNA.

If Figure 1 illustrates roughly how a device sizing and biasing can be selected for an optimum low noise design or moderately robust low noise device (red dotted section) or highly robust moderate noise device (blue dashed section), the trade-off between these HF noise and non-linear electrical characteristics can be difficult to manage during the initial selection of the transistor. In the next paragraph, we present two design strategies of the LNA for the best achievable low noise performances (HEMT 2), and for a moderate improvement of IP_{1dB} at the price of a slight noise factor degradation (HEMT 3).

A. Conventional Design method for LNAs

1) Methodology of design for $LNA_{\#1}$ and $LNA_{\#2}$

For $LNA_{\#1}$, we are only focusing on achieving the lowest noise figure $NF_{50\Omega}$ with an acceptable small-signal gain as the first amplification stage ($|S_{21}|$>10 dB). First, we focus on optimizing the active element. For this, we look at the figures of merit (NF_{min}, $\Delta NF=(NF_{50\Omega}-NF_{min})$, R_n, $|S_{21}|$ …). ΔNF represents the effort to design a Z_{IN}=50 Ω matched amplifier, also considering the noise mismatch. A transistor featuring 6 fingers, each of 40µm width, is selected at a biasing voltage of V_{GS}=-1V and V_{DS}=5V, with a reduced I_{DS} D.C current (I_{DS}=53 mA for a reduced shot noise, but still maintaining an elevated dynamic transconductance gain g_m). To achieve the terminals 50 Ω matching of the circuit, many combinations of input/output matching networks are tested (resp. IMN and OMN). First, lumped elements are used before replacing by their (R-)L-C equivalent elements from the Design Kit. Inductive serial feedback on the sources of the HEMT (north and south sides) allows the simultaneous efficient matching for the small-signal and noise reflection coefficients. In the end, a network with an inductance in parallel connected to the input of the HEMT, followed by a series capacitor was selected as an input matching network, which allows the best noise performance for this transistor. It also provides the bias tee at the MMIC level. Unconditionally stability is achieved at the end of the design process.

Concerning $LNA_{\#2}$, the same approach is used as with the $LNA_{\#1}$ except that P_{1dB} becomes a first order parameter just like $NF_{50\Omega}$. The objective is to improve by 9 dB the input compression point of $LNA_{\#1}$. From Figure 1, a bigger size of the transistor will be profitable for increasing its compression point, but the biasing I_{DS} current must remain low (very close to the pinch-off voltage) to master the noise degradation and to remain in a low noise amplification zone of Figure 1 (black zone). The HEMT is selected with 8x50µm size at a quiescent point of (V_{GS}=-1.25; V_{DS}=12V). Thus, the drain bias current is almost equivalent to the first $LNA_{\#1}$ with an I_{DS} set at 48 mA. Finally, the inductive feedback also has a strong influence on the gain. As stated in Figure 3, this will lead to a reduction in the small-signal gain $|S_{21}|$ while maintaining an acceptable $NF_{50\Omega}$ degradation, for the targeted P_{1dB}.

Electromagnetic simulations are performed to ensure good consistency between the electrical simulations, and to secure the characterization of the MMIC.

2) Simulated comparison between $LNA_{\#1}$ and $LNA_{\#2}$

The comparison of the simulated electrical and noise performances of the designed $LNA_{\#1}$ and $LNA_{\#2}$ is plotted in Figure 3. Obviously, selecting the best transistor only by considering the final noise figure (LNA#1, HEMT of 6x40µm)

Figure 2 : Device biasing and sizing selection for Low Noise or high compression IP1dB purposes (NFmin versus IP1dB @10 GHz). Sizing is for number of gate fingers and gate individual width respectively ranging between [2;4;6;8] and [20 µm to 100 µm by step of 20 µm], while biasing on V_{GS} and V_{DS} respectively range between [-1,7 V to 0 V by step of 0.2 V] and [3V;5V;8V;12V;20V]

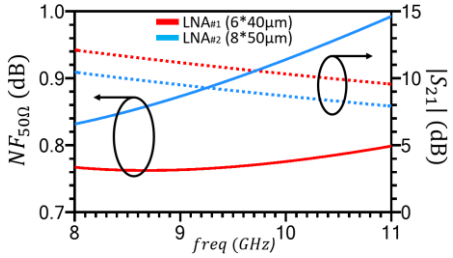

Figure 3 : 50 Ω Noise Figure ($NF_{50\Omega}$) and $|S_{21}|$ of $LNA_{\#1}$ (6*40µm) and $LNA_{\#2}$ (8*50µm) over the selected frequency bandwidth 8-11GHz

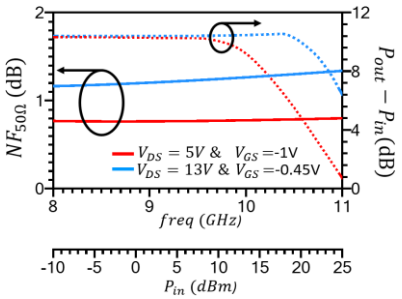

Figure 4 : Noise Figure (upper x-axis scale) and non-linear P_{out}/P_{in} (lower x-axis scale) of the $LNA_{\#tuned}$ in its low-noise nominal biasing mode (V_{GS}=-1V; V_{DS}=5V, same as for $LNA_{\#1}$) and in its electromagnetic-aggression protection biasing mode (V_{GS}=-0.45V; V_{DS}=13V).

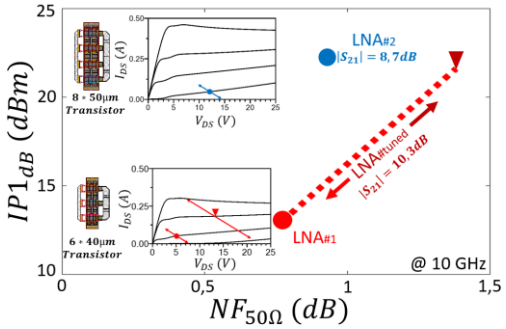

Figure 6 : Comparison between $LNA_{\#1}$ (low noise), $LNA_{\#2}$ (rugged) conventional designs and $LNA_{\#tuned}$ (reconfigurable both in noise and linearity).

gives the best achievable $NF_{50\Omega}$< 0.8 dB over 8-11GHz with a flat profile, and a small-signal gain $|S_{21}|$>9.5 dB while the reflexion parameters S_{11} & S_{22} are better than -12 dB.

However, as the non-linear elements have not been considered during the design process for $LNA_{\#1}$, the IP_{1dB} is simulated at 13 dBm which represent a good result regarding usual LNA circuits, but not enough high to protect against EM jamming signals. As $LNA_{\#2}$ results from a compromise between large-signal and noise design paradigms, the noise figure is not centered ($NF_{50\Omega}$ increases from 0.83 dB to 1 dB) but the IP_{1dB} is improved by 9 dB with IP_{1dB}=22.3 dBm at 10 GHz. This does not represent the maximum RF signal that the LNA can withstand [2] [3] , but the power for which the LNA is still operating in its linear regime, and for which detection is still possible. The linear gain is 2 dB lower than that of $LNA_{\#1}$, mainly due to the size and the biasing conditions of $LNA_{\#2}$, and also due to the chosen topology (feedback for better compression). Despite a slight degradation on the $NF_{50\Omega}$, $LNA_{\#2}$ represents an interesting alternative to $LNA_{\#1}$. But our objective is to design a Low Noise Amplifier able to provide the best $NF_{50\Omega}$ and also able to withstand elevated IP_{1dB}.

B. Original LNA design for reconfigurable $NF_{50\Omega}$ & IP_{1dB}.

This third and new approach to designing a robust LNA, intends to design an LNA that can be tuned from "low noise figure" to "high linearity" according to the incident input power level. It should be understood that the main constraint consists in keeping the layout of the circuit unchanged (i.e. the choice of the transistor and passive elements, therefore the topology of the circuit). Thus, only the quiescent point of the transistor can be used as a lever to satisfy this goal. Another important consideration is that the matching conditions must remain unchanged regardless of the biasing state of the transistor. The specifications are the same $NF_{50\Omega}$ as for $LNA_{\#1}$ (considered the best noise figure for an IP_{1dB}>12 dBm), and the same IP_{1dB}>22 dBm as for $LNA_{\#2}$ when the transistor is biased in its rugged configuration (but with a degraded $NF_{50\Omega}$).

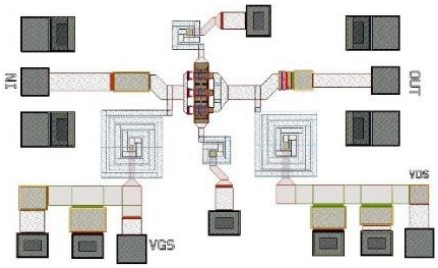

Figure 5 : Layout of the single-stage X-band $LNA_{\#tuned}$ MMIC

By using the same size of transistor as for $LNA_{\#1}$, it is found that a biasing of (V_{GS}; V_{DS}) tuned from (-1 V ;5 V) to (-0.45 V; 13 V) enables S_{11} and S_{22} of the HEMT to be stable, while NF_{min} and ΔNF degrade respectively by 0.5 dB and 0.3 dB and IP_{1dB} is improved by 9 dB as evidenced in Figure 4. It should be considered the elevated power dissipated while biased at V_{GS}=- 0.45 V under V_{DS}=13 V, with a dissipated power of 4.1W/mm, close to the maximum rating, but this state is only used for limited short time period under jamming signal.

Obviously, the unconditional stability should be satisfied for each biasing conditions, as well as along the biasing path between these two quiescent states. The final layout of $LNA_{\#tuned}$ is represented in Figure 5. To support the proposed study, nonlinear and noise electrical measurements will be presented, as well as the multi-stage LNAs, at the conference. Figure 6 represents the IP_{1dB} versus $NF_{50\Omega}$ at 10 GHz for the three LNAs, with their associated biasing. The two states of $LNA_{\#tuned}$ testify to the great flexibility of the performances of a same and unique circuit. This new reconfigurable LNA is compared with $LNA_{\#2}$. The output characteristics, the layout of the selected transistors or the different biasing conditions are reported for a better understanding of the potential of the proposed strategy.

III. Conclusions

For the first time, a reconfigurable GaN MMIC LNA is presented which allows the electrical and noise performance of a LNA to be changed from low-noise behavior to a rugged highly linear amplifier, in a perfectly reversible manner depending on the applied D.C bias. Three different strategies can be developed according to the case of study of the receiver:

-if the receiver does not need to prevent RF signals higher than 13 dBm at its input, $LNA_{\#1}$ can be used as it is.

-if the receiver must withstand high input RF signal (jamming) but still maintaining acceptable noise figure, $LNA_{\#2}$ presents a good alternative to $LNA_{\#1}$.

-if the front-end needs to operate at its best noise figure under nominal operational mode (no jamming signal), but also needs to be protected from EM aggression while still maintaining its operability in linear condition, then $LNA_{\#tuned}$

provides the designer with not yet available MMIC LNA circuits (layout in Figure 5).

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