A x3 Sub-Sampling Mixer for a 77 GHz Automotive Radar Receiver in 28 nm FD-SOI CMOS Technology

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***Abstract* — This paper presents an innovative x3 sub-sampling frequency downconverter for converting signals around 77 GHz from a 26 GHz LO signal. With a LO frequency divided by 3 this topology allows drastic simplifications on the receiver's LO distribution chain. The sub-sampling mixer operation principle is described and implemented with 28-nm FD-SOI CMOS technology. Simulation results show a 1dB input-referred compression power (ICP1dB) of +3 dBm and a 14.4 dB Noise Figure (NF) with a -2.5 dB conversion gain. The mixer's LO signal shaper consumption is 36 mW on a 1.2V supply while the passive mixer core doesn't require DC power.**

***Index Terms* — Millimeter-wave, Sub-harmonic, Passive mixer, Frequency down-conversion, Low duty cycle.**

I. INTRODUCTION

With its ability to detect distant targets under harsh visibility conditions, the 77 GHz automotive radar plays a key role in driving safety. Using high frequencies enables a good circuit integration and a fine range resolution thanks to a wide modulation bandwidth. Nevertheless, implementing a 77 GHz LO chain to drive the mixer is difficult as it generally requires a 38.5 GHz VCO, frequency doublers and high consumption 77 GHz amplifying stages.

A solution to overcome difficulty coming with this complexity could be found with sub-harmonic mixers that use a LO frequency submultiple of the RF frequency ($f_{LO} \approx \frac{f_{RF}}{n}$, with n a natural integer). This solution has already been considered for the first generations of 77 GHz radar receivers ([1],[2]). However, as sub-harmonic passive mixers often result in prohibitive conversion losses, the high-frequency architectures mostly rely on sub-harmonic active mixers. At lower frequencies, passive sub-sampling mixers as in [3] are widespread. As this principle translates into low conversion losses and good linearity, the aim of this paper is to demonstrate that it can be applied to millimeter-wave frequencies. So, a ×3 sub-sampling passive mixer is proposed in this paper for a 77 GHz radar receiver.

Section II introduces the sub-sampling mixer principle. Then, the proposed topology is detailed in section III with a focus on its innovative mixer core and the associated 26 GHz LO signal shaping method. The implementation with the 28 nm FD-SOI CMOS technology and the simulation results are given in section IV. Finally, the conclusions of this work are presented in section V.

II. SUB-SAMPLING MIXER PRINCIPLE

In an ideal sub-sampling operation, every RF signal close to any sampling frequency harmonic ($n.f_{LO}$) is translated at $f_{FI} = |f_{RF} - n.f_{LO}|$ with a 0 dB conversion gain. The sub-sampling operation is particularly interesting because it allows a theoretically lossless frequency conversion from any LO frequency such as: $n.f_{LO} \approx f_{RF}$.

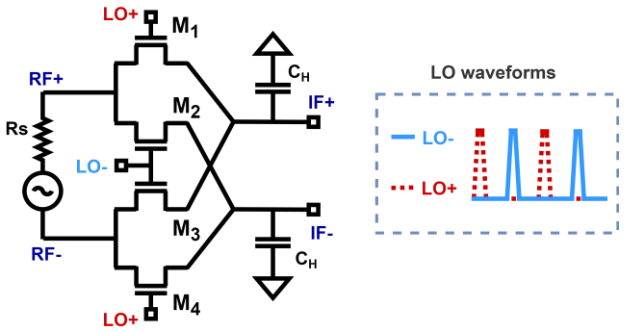

Figure 1: sub-sampling mixer topology

The sub-sampling mixer principle is described with a double-balanced topology in fig.1. Applying a low duty cycle square wave as LO signal and presenting a capacitive load at the IF outputs turn the mixer into a voltage sampler. Transistors are used as switches closed for a very short time to sample the input voltage. Sampled values are stored by the hold capacitors C_H when all the switches are open. The mixer brings a high input impedance around each odd LO harmonics ($n.f_{LO}$) enabling a proper voltage conversion as soon as source impedance is low enough ($R_s \ll Z_{in}$). If $D.T_{LO}$ defines the $M_{1,2,3,4}$ conducting time, the passive sub-sampling mixer's voltage conversion gain (G_{cv}) calculation gives, with a similar approach as in [4]:

$$G_{cv} = \frac{1}{2} sinc(\mathrm{n}.D)(1 - e^{-j\pi n}) \quad (1)$$

According to (1), for odd values of n, the subharmonic frequency conversion can be achieved with low loss if D can be small enough.

In addition, this sub-sampling mixer benefits from the passive mixer's linearity performances that can be excellent if transistors switching time is low [5]. Consequently, with sharp

LO signal's rising and falling edges, this mixer will be highly linear.

However, at millimeter-wave frequencies, the possible choices for *n* are limited. The equation (1) shows that the more *n* increases the more *D* must be kept low to reach a decent conversion gain. As low duty cycles are difficult to reach at high frequencies, the higher reasonable ratio *n* appears to be 3 for a 77 GHz sub-sampling operation. So, a 26 GHz LO frequency has been chosen for the implementation of the 77 GHz sub-sampling mixer.

The following section demonstrates that designing a LO shaping circuit for the creation of a 26 GHz pulsed signal becomes feasible by taking advantage of nm-scaled CMOS processes. This design is addressed in the next section.

III. CIRCUIT DESCRIPTION

Even if nm-scaled CMOS technologies provides high speed transistors, their gate capacitances and parasitic elements limits the high frequency gain of complex logic gates. Nevertheless, the generation of a low duty cycle LO signal only requires inverter chains to generate two time-delayed square waveforms and an AND gate for their combining. So, using only these logic gates can be compliant with the need of a proper 26 GHz pulse shaping.

In the inverter/AND gate arrangement, the AND gate is the limiting element because of its complexity. Thus, the reachable duty Cycle is not low enough. To overcome this limitation the AND function has been merged with the mixer core, as depicted in fig.2

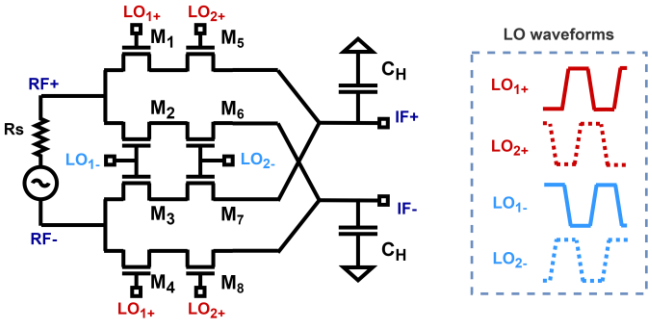

Figure 2: Mixer core with the co-integration of the AND gates

The operating principle of this mixer core and the one described in fig 1, stays similar. LO_2 is a delayed version of LO_1. For example, in fig.2, series transistors M_1 and M_5 are both open only when LO_{1+} and LO_{2+} are simultaneously at the high state. This operation is equivalent to a single transistor driven with a pulsed LO signal with a duty cycle $D = \frac{t_{LO_{1+} \cap LO_{2+}}}{T_{LO}}$ where $t_{LO_{1+} \cap LO_{2+}}$ is the LO_{1+} and LO_{2+} intersection time.

This innovative approach allows to suppress the AND gates to reach lower duty cycles and sharper LO signal's edges. As a result, only inverter chains are needed to generate the required LO waveforms for the sub-sampling mixer core. Nevertheless, since two series transistors are involved in each branch of the mixer, this topology presents a higher ON-state resistor (r_{on}), increasing the thermal noise.

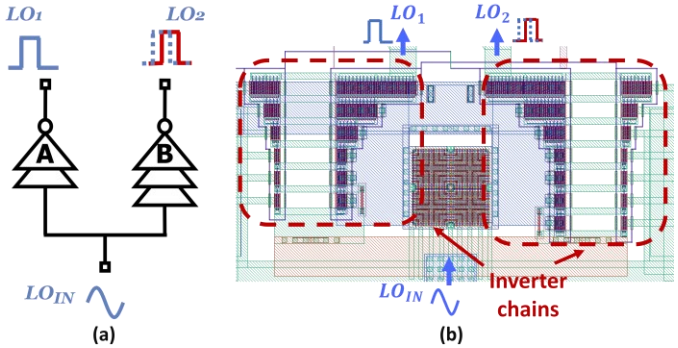

Figure 3: (a) single ended LO signal shaper (b) Signal shaper's layout

Fig.3 presents the single ended version of the LO signal shaper. In the proposed mixer architecture, this structure is duplicated and fed with an opposite phase sinusoidal signal to implement a differential LO signal shaper. The LO signal shaper's layout of fig.3.b shows that the transistor size is progressively increased along the inverter chains. This way, current capability of inverters is progressively increased until the required value for a proper driving of the mixer.

In the LO signal shaper, the inverter chains A and B have a different number of stages to create the required time delay between both square signals. The body effect of FD-SOI technologies is quite high (~ 85 mV/V), so that the body voltage can be changed to tune the V_{th} of transistors. This property is used in this LO signal shaper to provide an additional LO duty cycle tuning capability. In each inverter, applying a tuning voltage V_{tune} at the NMOS transistor body and $-V_{tune}$ at the PMOS transistor body creates a V_{th} shift resulting in a different inverter's time delay. Finally, changing the delay between the square signals before the mixer directly changes the LO duty cycle *D*. Tunning voltage's values of opposite sign are chosen for the inverter chains A and B to increase the duty cycle tuning range.

The overall mixer architecture and the corresponding layout are given in fig.4.

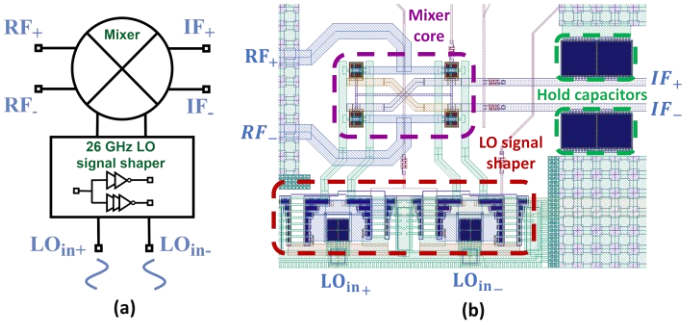

Figure 4: (a) Sub-sampling mixer architecture (b) Mixer's layout

The mixing transistor sizing is essential to get a good noise/linearity trade-off. To get the best linearity from the sub-sampling mixer, sharp LO square signal's rising and falling edges are needed. Since the capacitive load of transistor gate contributes to soften the LO square voltage edges, a lower width of transistor lead to a better linearity. On the other hand, increasing the width helps to keep a low NF by lowering the series resistance r_{on}. The resulting transistor sizing is 20 µm/30 nm.

Implementation and simulation of the sub-sampling passive mixer topology is detailed in the following section.

IV. IMPLEMENTATION AND SIMULATION RESULTS

The 77 GHz sub-sampling passive mixer is designed in a 28-nm FD-SOI CMOS process from STMicroelectronics.

The LO signal shaper supply voltage is $V_{DD} = 1.2V$. This value satisfies a trade-off between the necessary LO swing to get a good mixer's linearity, the LO signal shaper's consumption and the transistor's reliability. In an inverter the transistors never experience high V_{gs} and high V_{ds} at the same time making it less sensitive to Hot Carrier Injection, even with 1.2V supply voltage. Fig.5 shows the output voltages of the A and B inverter chains (fig.3).

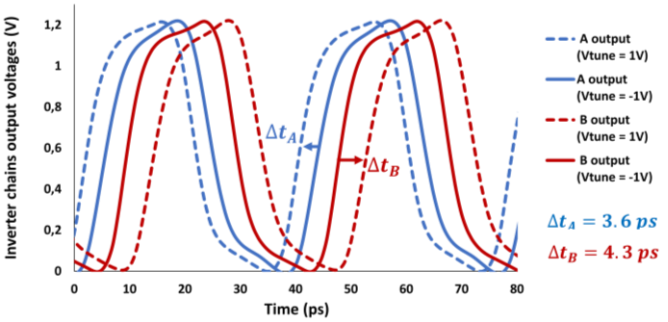

Figure 5: Inverter chains output voltages

Solid line and dot line waveforms correspond respectively to the minimum and the maximum time delay between A and B output signals. The maximum achievable time delay variation is $\Delta t_{MAX} = \Delta t_A + \Delta t_B = 7.9\ ps = 0.2 \times f_{LO}$ and is obtained with V_{tune} varying in the range [-1V, +1V]. The LO signal shaping DC power consumption is 36 mW.

Harmonic-balance simulation results, with $f_{RF} = 78.02\ GHz$, $f_{LO} = 26\ GHz$ and $f_{IF} = 20\ MHz$, are reported in fig.6. This simulation is based on a layout modelling using momentum and a Post Layout Simulation extract.

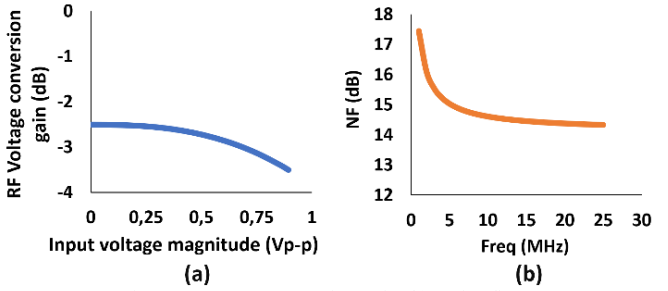

Figure 6: (a) RF conversion gain (b) Noise figure.

The simulated voltage conversion gain is depicted in Fig6.a. Under these conditions, the sub-sampling mixer has a simulated conversion gain of -2.5 dB. The input -1 dB compression voltage $V_{\text{-1dB}}$ is 0.9 V_{p-p}. Power is not used here to express mixer performance as it is not relevant regarding the high Z_{in} of the mixer. An equivalent ICP1dB of +3 dBm is derived considering that $V_{\text{-1dB}}$ is delivered to a 50 Ω load.

Results of a non-linear noise simulation based on harmonic balance are presented in fig.6.b. The NF simulated with a 50 Ω input port is 14.4 dB at a 20 MHz IF frequency.

The proposed sub-harmonic passive mixer has been implemented with a variation of the LNA presented in [6] in a 77 GHz front end. The simulated front end's performances are summarized and compared with other radar receivers in table 1.

TABLE 1: FRONT-END'S SIMULATED PERFORMANCES AND COMPARISON

	Tech	f_{RF}/f_{LO} [GHz]	G [dB]	ICP1dB [dBm]	NF [dB]	DC Power [mW]
LNA + this work	28 nm FD-SOI CMOS	78/26	10.2	-10	11.5	36 + 9 Mixer + [6]
[1]	65 nm CMOS	77/38.5	16	-20	10.5	57
[2]	65 nm CMOS	77/38.5	16	-20	13	28.5

The simulated performances show that with a high linearity, a good conversion gain and a higher $\frac{f_{RF}}{f_{LO}}$ ratio the proposed mixer appears as a favourable alternative to [1] and [2].

Furthermore, with the proposed solution a 26 GHz VCO can be used without multiplying stages. The 26 GHz LO signal amplification also consumes less DC power than at 77 GHz. And finally, the logical gate LO signal shaper enables a very compact design as it does not require transformers or inductors.

V. CONCLUSION

A x3 sub-sampling passive mixer topology operating at 77 GHz with a 26 GHz LO signal frequency is proposed in this paper. This solution is based on an innovative sub-sampling mixer core associated to a 26 GHz LO signal shaper.

The sub-sampling principle allows to design sub-harmonic passive mixers benefiting from good linearity while keeping a good conversion gain. This approach also gives the opportunity to significantly simplify the LO chain from the division by 3 of the LO frequency. According to these results, the proposed architecture demonstrates that the sub-sampling mixers can be convenient to address millimeter-wave frequency applications.

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