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A Comparative Study of DPI levels on BMS IC With an On-Hand Analytical Model to Predict Resonances

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Abstract— When it comes to the electromagnetic interference (EMI) immunity of a Battery Management System Integrated Circuit (BMS IC), Printed Circuit Board (PCB) traces, external components and BMS impedance have a major impact. In a number of cases, electromagnetic compatibility (EMC) issues are reported at the last testing phase which can lead to design changes thus increasing cost and time to market. In this context, this work gives an insight on what some design choices on the external components, PCB traces and hot-plug (HP) protection architecture can lead to in terms of the noise coupled to the BMS IC. Moreover, an analytical model based on ladder network theory is used to predict the main noise coupling frequencies under some low-cost design choices. This model is then used in the comparison of two HP protection architectures in terms of the noise coupled onto the BMS IC.

Keywords— BMS; PCB; Battery; High Frequency; DPI; Resonance; Noise levels; Hot-Plug; Ladder Networks.

I. INTRODUCTION

Lithium Ion (Li-Ion) batteries as well as BMS [1] have been subject to extensive research to pave the way for the new generation of Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV). One major aspect of development, for example, is the characterization of the conducted EMI coming from the drive inverter [2] which is one of the noise sources that can act as an aggressor to the BMS integrated circuit (IC). In this noise path the PCB traces and BMS impedance highly contribute to the correct assessment of the incoming noise spectrum. While a number of articles [2][3] deal with the later point, this article investigates the effect of those components during EMC simulations of the BMS IC. Indeed, during the design flow of the BMS IC, the simulation of standard EMC immunity tests such as direct power injection (DPI) [6] is performed along the way to evaluate the immunity of the IC and perform design changes and optimizations prior to the test phase in order to anticipate as many issues as possible, thus, a faster time to market. Therefore, choosing the right model for the BMS front end plays a major role in the noise injection levels. More importantly, the configuration by which some of the external components are connected directly alters the noise coupling frequencies, e.g. the HP protection capacitors. Therefore, having an on-hand simple predictive model of the main noise coupling frequencies and injection levels in the early design stages can be vital for both properly characterizing and improving the immunity levels of the BMS IC and optimizing external Bill Of Material (BOM) such as filters, protection capacitor, etc. Indeed, while ladder networks theory has already been thought of as a way to approach

transmission lines [4], this work uses it to build a simple approach to extract the main noise coupling frequencies in a BMS environment.

On the BMS IC side, the integrated HP protection diodes also contribute to the presented impedance, thus influencing the DPI injection levels. Besides, the capacitive effect of these diodes affects the IC's impedance in different manners depending on the HP protection architecture. Two main architectures are distinguished: a centralized architecture [8] and a differential one [7]. Therefore, having an on-hand analytical model for predicting the maximum noise coupling frequencies during DPI with the inclusion of the HP protection can be crucial in the early design steps. It does not only helps in choosing the appropriate HP protection architecture in terms of injection levels, but also gives design guidelines on such architecture to reduce the coupled noise. In this work, such a model is proposed, validated by simulations and used to back the comparison between the two HP protection architectures in terms of maximum coupled noise.

Finally, the goal of this article can be summarized as follows:

- Provide a simple modeling approach of the BMS itself and its environment during DPI simulations as well as a predictive analytical model of the main coupling frequencies depending on the configuration of the external HP capacitor.
- Compare two HP protection architectures in terms of DPI injection levels along with providing an analytical predictive model that predicts the main noise coupling frequencies along with validating the comparison results.

This paper is organized as follows: First, some basic notions of the BMS IC front end will be given. Secondly, the considered models for each of the PCB traces, BMS IC and DPI injection will be presented. Thirdly, the effect of the HP capacitor configuration on the coupled noise is investigated and an analytical model for resonance frequencies prediction is elaborated. Then, the comparison between the two HP protection architectures is presented along with the analytical model.

II. TYPICAL BMS IC FRONT END

The main purpose of a BMS is to ensure the proper and safe operation of the battery especially with Li-Ion chemistry-based batteries which have to operate under a certain

temperature and voltage range. Some of the main functions of a BMS are to perform accurate cell voltage measurement and passive cell balancing [1] to prevent cell degradation and enable optimum power extraction from the battery pack. Fig. 1 shows a high-level diagram of the BMS front-end and surrounding external environment, where S_i are the balancing switches, C_d are an HP protection capacitors (47 nF), and R_b are the balancing resistors.

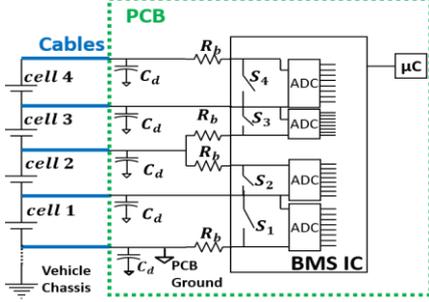


Fig. 1. Typical high-level view of a BMS IC front end

III. MODELING OF THE BMS ‘CHAIN’ APPLICATION

The goal of this section is to elaborate models of the battery, PCB and BMS IC which are crucial to run reliable DPI simulations on one hand but also to pave the way to a simple analytical approach to predict the injection levels as well as the main noise coupling frequencies.

A. BMS IC Model

In order to simplify this approach, the main contributor to the impedance presented by the BMS IC is considered to be the cell balancing switch. Indeed, these switches are designed to have a large area and minimum heat dissipation in the IC during passive cell balancing, and thus present a relatively considerable equivalent capacitor value when they are open. By simulating the parasitic capacitances of an existing switch design, an ideal capacitor C_L of 30 pF was chosen as a representation.

B. PCB Traces and DPI Model

In Fig. 1, the PCB traces is modeled depending on the considered length. Knowing that the maximum length belongs to the battery cables (in blue in Fig. 1) which is 20 cm, a simple lumped model could be used to model the traces and cables. With the presence of capacitor C_d (47 nF) and R_b with a value of 15 Ω , the capacitive and resistive effects of the cable and traces models is neglected. Thus, only inductors are used to model the cables as well as the sectioned traces with values depending on the length. L_0 in Fig. 2 models the battery cable (200 nH) while L_1 models different sections of the PCB traces. In addition, a realistic model of capacitor C_d is used as it includes its equivalent series inductance and resistance behavior. When it comes to DPI, it is implemented in common mode way where 30 dBm (V_i in Fig.2) is coupled to the PCB traces through R_i and C_i (6.8nF) as the standards require. Due to the values of L_0 and C_d , the frequency range of interest will be [150 kHz; 100 MHz], for now, as the introduced resonances from L_0 and C_d will be within that range.

Based on the setup of Fig. 2, two configurations will be presented to compare the corresponding injection levels:

- Config A: C_d connected to ground.
- Config B: C_d connected differentially (Fig.2).

Finally, in order to extract the peak-to-peak differential voltage across the load capacitors, transient simulations were performed in SPICE environment for 4 cells where:

- The simulation was given enough periods for the signals to settle (above 500 periods) before extracting any data.
- The peak-to-peak voltages, denoted as $V_{pk2pk}(C_{Li})$, for each injected frequency were extracted as an average on the data of the last 50 periods of the signal.
- Lastly, a sufficient numbers of points per decades were taken in the range of [150 kHz; 100 MHz] (500 pts/decades).

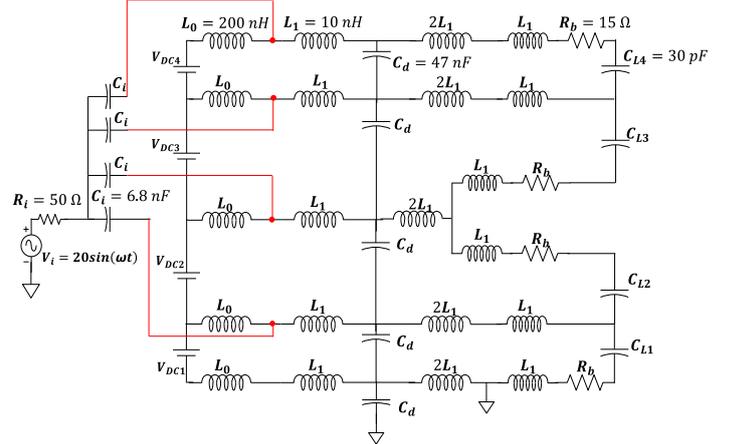


Fig. 2. Modeling of the PCB traces and DPI CM injection for Config B.

In the following section, the simulation results will be shown and compared.

IV. EFFECTS OF CAPACITOR C_d CONFIGURATION ON DPI INJECTION LEVELS AND ANALYTICAL MODEL

In this section, the comparison will be elaborated between config A and config B in terms of the peak-to-peak value of the differential voltage generated across the load capacitors C_{L1} , C_{L2} , C_{L3} and C_{L4} . This value will be denoted as $V_{pk2pk}(C_{Li})$. Then an analytical model based on ladder networks theory is presented to predict the maximum noise coupling frequencies.

A. Simulation Results

When C_d is connected to the ground (config A), the PCB traces layout presents a symmetrical impedance on each branch. Since the DPI is performed in a common mode way, minimal common mode to differential conversion is expected. Indeed, Fig.3b,3c,3d show that config A displays a considerably lower injection level. For the bottom cell in config A, since one of the branches is connected to the ground, the DPI injection is virtually differential, thus presenting a higher injection level than the other cells. When it comes to config B, placing C_d differentially would lead to a relatively higher common to differential mode conversion. In fact, as seen in Fig.3, resonance frequencies are introduced due to coupling between the different branches of the PCB. Therefore, additional frequencies where the BMS IC might be susceptible are present. Furthermore, while config A allows for lower injection levels and number of resonance frequencies, the capacitor C_d itself would have to be rated for a high voltage as it is connected to the ground. Therefore, config A implies a higher capacitor C_d price especially in a pack that has a high number of battery cells. On the other hand,

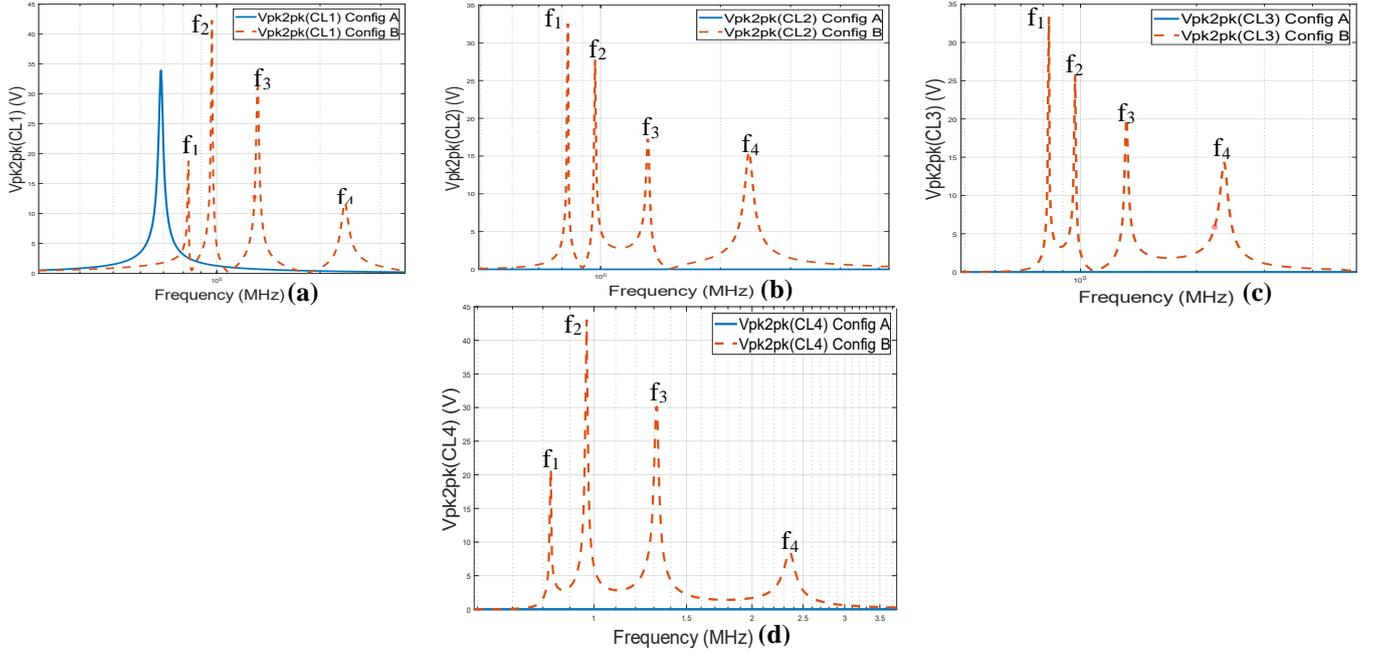


Fig. 3 $V_{pk2pk}(C_{L_i})$ simulation results as a function of the injected frequency and comparing Config A with B. In the exception of the shown frequency range, the two curves of each graph fit together. (a) $V_{pk2pk}(C_{L1})$ in Config A and B. (b) $V_{pk2pk}(C_{L2})$ in Config A and B. (c) $V_{pk2pk}(C_{L3})$ in Config A and B. (d) $V_{pk2pk}(C_{L4})$ in Config A and B.

config B leads to higher injection levels and more importantly to the introduction of maximum noise coupling frequencies. However, since C_d is placed differentially, it is rated for a much lower voltage, yielding a lower price. Since config B implies the cheapest choice, an analytical model for predicting the maximum noise coupling frequencies based on ladder networks is elaborated in the next section.

B. Analytical Model of Maximum Noise Coupling Frequencies

In order to approach a simple analytical model, some considerations are made in the case of Config B (Fig. 2). First, in the context of config B and due to the high ratio between C_d and C_L , the effect of the BMS IC could be neglected in frequencies lower than 100 MHz. Secondly, since the ideal voltage source doesn't present any sort of impedance, it could be considered as a short for AC calculations. Fig. 4 illustrates the model. Furthermore, in order to ease the approach, a differential DPI injection setup on the up most PCB trace is considered as shown in Fig. 6a.

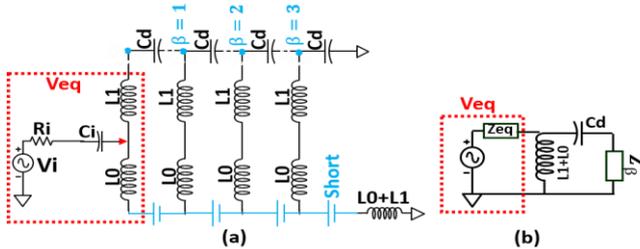


Fig. 4. Simplification of PCB model from Config B. (a) removal of C_L and R_b . (b) simplified model using Z_β

From Fig. 4a, the PCB traces model now is a C-L ladder network with an input V_{eq} . The considered outputs in this case are the differential voltages across capacitors C_d . Based on [4], the following equation gives a first simple approximation to the injection levels:

$$V(C_d) = \frac{\sum_{j=0}^{n-\beta+1} c_{j,n-\beta+1} \left(\frac{1}{s^2(L_0+L_1)C_d} \right)^{j+1}}{\sum_{j=0}^n b_{j,n} \left(\frac{1}{s^2(L_0+L_1)C_d} \right)^j} V_{eq} \quad (1)$$

Where $C_{j,n-\beta+1}$ and $b_{j,n}$ are a function of the binomial coefficients [5] and β is the node of interest (Fig. 4a). More interestingly, in order to prove (1), a recursive formula of the impedance seen from any node β to the right between different nodes has to be elaborated. Such an impedance is written as follows [5].

$$Z_\beta(s) = \frac{\sum_{j=0}^{n-\beta} b_{n-\beta,j} \left(\frac{1}{s^2(L_0+L_1)C_d} \right)^j}{\sum_{j=0}^{n-\beta+1} c_{n-\beta+1,j} \left(\frac{1}{s^2(L_0+L_1)C_d} \right)^{j+1}} \quad (2)$$

Using (2), the PCB traces in Fig. 4a can be simplified as in Fig. 4b when $\beta=1$. From Fig. 6b, maximum noise coupling occurs when the impedance reaches a maximum value. Under this condition, Z_β is maximum for these frequencies. Based on [4], the roots of the denominator of (2). can be written as the following for $\beta=1$:

$$f_{N_{cells}}^{(i)} = \frac{1}{4\pi\sqrt{(L_0+L_1)C_d} \sin\left(\frac{i}{2(N_{cells}-\beta+2)}\pi\right)} \quad (3)$$

Where N_{cells} is the number of cells in the pack and 'i' is the index of the resonance frequency which is included in [1; N_{cells}]. In order to validate the previous equation, the four resonance frequencies were calculated and compared with their respective simulated values from Fig. 5e,f,g,h (under Config B).

TABLE 1. Calculated and simulated resonance frequencies.

	Config B Simulation	Equation (3)
f_1	826.116 kHz	842 kHz
f_2	968.481 kHz	990 kHz
f_3	1.319 MHz	1.36 MHz
f_4	2.366 MHz	2.59 MHz

From Table.1, the simulated resonance frequencies (with the full PCB traces model in Fig.2) are close to the calculated values (difference less than 10%). This confirms, to some extent, the set of considerations that were made in the beginning of this section. Therefore, one could directly predict the set of maximum noise coupling frequencies if some capacitors are to be connected differentially between the PCB traces. Moreover, it allows to predict the effects of some PCB layout choices on the coupled noise in the early design stages. Finally, config B will be retained for the rest of the article as it presents the lowest cost approach in terms of the capacitor price. Next, the inclusion of the HP protection architecture will be elaborated.

V. COMPARISON BETWEEN THE HOT-PLUG PROTECTION ARCHITECTURES IN TERMS OF DPI INJECTION LEVELS AND ANALYTICAL MODELS

While the HP protection is supposed to be activated in an HP event to redirect the inrush current to the ground depending on which BMS IC pin is first connected to the pack, it is designed not to do so when subjected to DPI. However the capacitive effect of the diodes still has an impact on the immunity level of the BMS IC. In this section, a high frequency (HF) model of the HP protection diodes is elaborated and validated by simulations first, then, the comparison between the two HP protection architecture is presented alongside different cases of balancing resistor values (R_b).

A. Diodes HF Model

In order to take advantage of the ladder networks analytical approach used in the previous section, an HF model of the diodes needs to be considered for the calculations.

1) Centralized Architecture

The centralized architecture [8] makes use of diodes to redirect the inrush current toward a single centralized ESD clamp. Fig.5a. displays the considered architecture:

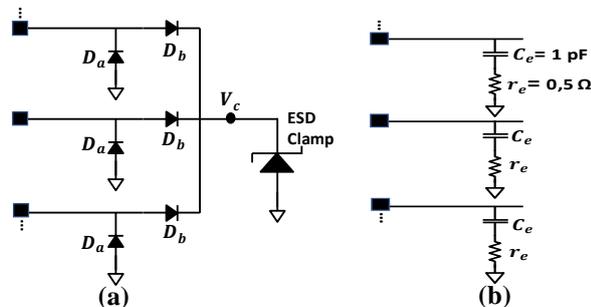


Fig. 5. (a) Centralized HP protection architecture.(b) High frequency model of the centralized HP protection architecture

Relative to [8], diodes D_a were added for a more realistic approach, in case some of the branches drop to negative values. Moreover, the V_c node is biased around the pack voltage, therefore, when going from one cell to the upper one, the voltage across D_a increases and the voltage across D_b decreases. Since the junction capacitance of the diode is inversely proportional to the reverse voltage across it, D_a will present a lower capacitance and D_b a higher capacitance as one goes up the battery pack. The ESD clamp on the other hand presents a much higher capacitance than D_a and D_b directly to the ground. Additionally, the diodes present a small resistance due to the quasi-neutral region which is present in the AC signal path. Fig.5b displays the considered model.

In order to validate this model, DPI simulations were performed with only 15 dBm as injection level to prevent D_a at the lowest cell from clamping, thus maintaining a capacitive effect. 18 cells were considered with the centralized architecture on one hand and with the model on another hand without the inclusion of R_b in order to see all of the resonance frequencies in [150 kHz; 1 GHz]. Transient simulations were used with 1000 points per decades.

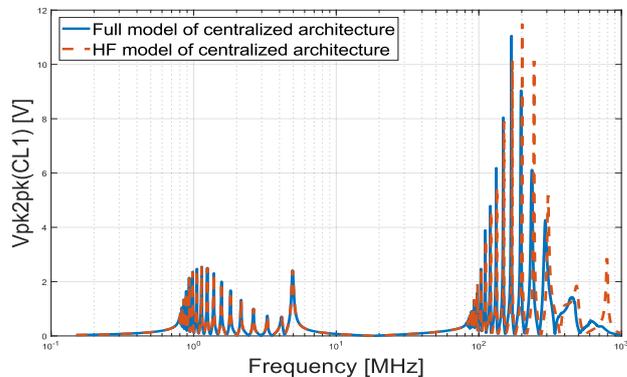


Fig. 6. Centralized architecture high frequency model validation.

From Fig.6, the HF model shows good agreement with the simulated architecture and thus will be retained for further calculations. Finally, since the low frequency resonances are caused by C_d as shown in the previous section, the high frequency resonances are generated by $\{3L_1, C_L\}$ C-L ladder network due to relatively lower inductance and capacitance values. Thus, further simulations will be performed in the [70 MHz ; 1 GHz] range.

2) Differential Architecture

The differential architecture in [7][8] relies on differential Zener diodes to diverge the inrush current towards the ground. Similarly to the centralized architecture, the following model was proposed.

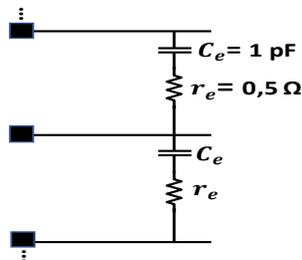


Fig. 7. High frequency model of the differential HP protection architecture

The differential architecture model was validated in the same way as the centralized one in the [70 MHz; 1GHz] range.

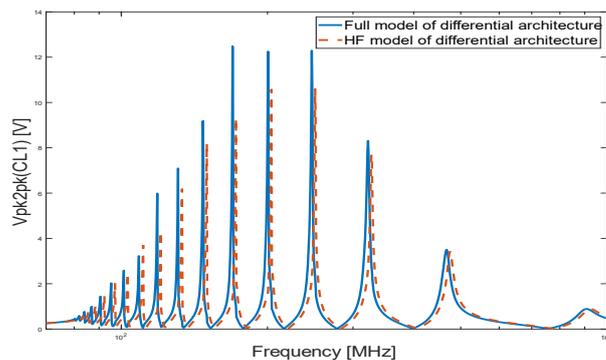


Fig. 8. Differential architecture high frequency model validation.

From Fig.8, the model shows good agreement with the simulated architecture and thus will be kept for further calculations.

B. Comparison Between The Centralized and Differential Architectures Without R_b

In order to effectively visualize the effect of each HP protection architecture, R_b is removed first. For a simpler approach the PCB traces layout is considered as in Fig.9 for 18 cells. DPI simulations were performed with both the centralized and differential HP protection architecture. Transient simulations were used to extract the peak-to-peak voltage with 1000 points per decades.

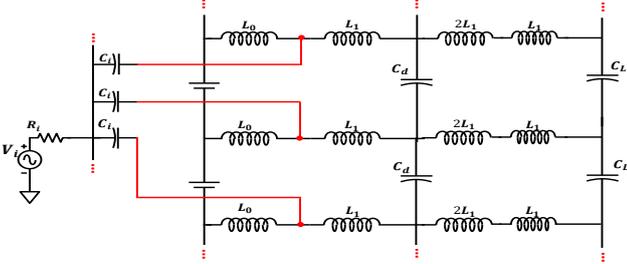


Fig. 9. PCB traces layout considered in the simulation for the comparison of the two architectures for 18 cells.

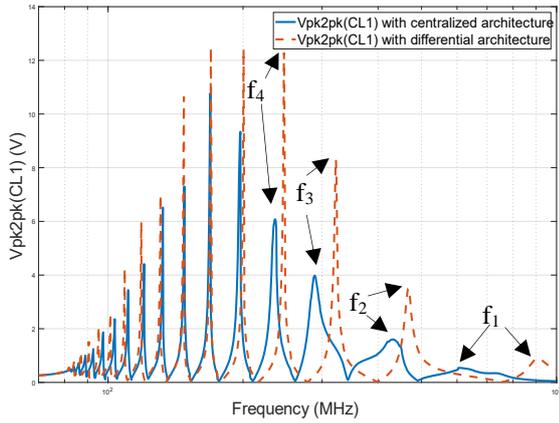


Fig. 10. Comparison between the two HP protection architectures in terms of injection levels onto C_{L1} without R_b .

From Fig.10, the centralized architecture leads to a lower injection level more importantly in higher frequencies starting from f_4 to f_1 . Additionally, the centralized architecture displays a higher frequency shift than the differential one at higher frequencies (f_4 , f_3 , f_2 , f_1). As additional validation, the simplification approach performed in the previous section will now be done in the presence of both the centralized and differential HP protection architectures. Since the high frequency resonances are now of interest, C_d displays a very low impedance and can be considered as a short leading to the following ladder networks.

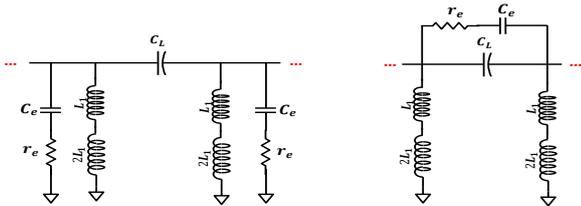


Fig. 11. Approximated PCB traces model with the inclusion of the models of the HP protection architectures. (a) centralized architecture. (b) differential architecture.

In order to first extract the resonances frequencies, equation (2) is expressed in the case of Fig.11a and Fig.11b. Extracting the resonance frequencies amounts to finding the roots of the following polynomials:

- In the case of the centralized architecture:

$$D(s) = 1 + C_e r_e s + 3L_1(C_e + a_{n,i}C_L)s^3 + a_{n,i}C_L 3L_1 C_e r_e s^3 \quad (4)$$

Where “ i ” is the resonances frequency index $a_{n,i} = 4 \sin\left(\frac{i}{2(N_{cell}-\beta+2)}\pi\right)^2$, $\beta = 1$, and $N_{cell} = 18$.

- In the case of the differential architecture:

$$D(s) = 1 + C_e r_e s + 3L_1 a_{n,i}(C_e + C_L)s^3 + a_{n,i}C_L 3L_1 C_e r_e s^3 \quad (5)$$

Where “ i ” is the resonances frequency index, $a_{n,i} = 4 \sin\left(\frac{i}{2(N_{cell}-\beta+2)}\pi\right)^2$, $\beta = 1$, and $N_{cell} = 18$.

Each of these polynomials has 3 roots where one is real and the two others are complex conjugates. The real roots are poles that are present in the THz frequencies introduced by the HP protection architectures. However, the complex roots directly reflect the resonances of the ladder networks in Fig.11. More precisely, the real part of these complex roots is the signal attenuation, i.e. the higher the absolute value of the real part, the higher attenuation level. As for the imaginary part of the complex roots, it represents the resonance frequency itself. For the frequencies of interest, their predicted value by the model is shown in Table.2.

TABLE 2. Calculated and simulated values of f_1 , f_2 , f_3 , f_4 .

	Centralized		Differential	
	Simulated [MHz]	Equation (4) [MHz]	Simulated [MHz]	Equation (5) [MHz]
f_4	236.1	248.695	246.7	254.136
f_3	289.1	320.271	322.2	336.142
f_2	433.6	445.672	466.8	501.340
f_1	613.9	682.434	920.7	999.257

As can be seen from Table 2, the model shows fair prediction of the resonance frequencies. Moreover, it only confirms that the centralized architecture places resonances at lower frequencies than the differential one. This analytical approach can be used in early design stages to easily determine the effect of each of the PCB traces layout and HP protection architecture. Moreover, it can help predict the frequencies for which the IC could be more susceptible in the early design stages. When it comes to the real part of the complex root, Fig.12 compares the calculated attenuation level of both the centralized and differential architectures.

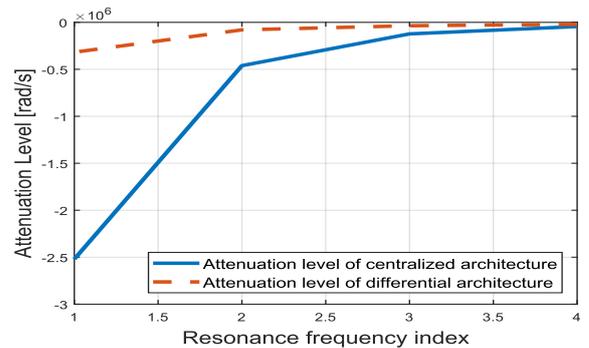


Fig. 12. Comparison of the attenuation levels of the differential and centralized HP protection architectures.

Fig.12 shows that the centralized architecture inherently provides a higher attenuation for the higher frequency resonances than the differential architecture. Next, R_b is added and the comparison between the two architectures is presented.

C. Comparison Between The Centralized and Differential Architecture With R_b Included

With the inclusion of R_b , a more realistic case of injection level is obtained. R_b is then included on each PCB traces branch in Fig.9 with a value of 7.5Ω . While R_b is now the primary source of power dissipation, the comparison of the two architectures in terms injection levels is carried out in Fig.13.

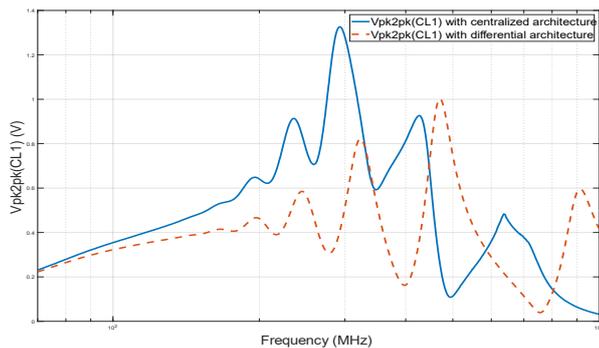


Fig. 13. Comparison between of the two HP protection architectures in terms of injection levels onto C_{L1} with R_b .

From Fig.13 the centralized architecture displays lower injection levels towards the higher frequencies and higher shift to lower frequencies than the differential one. However, a slight increase is shown around 260 MHz. When R_b is reintroduced, the quality factor of the resonance frequencies is drastically reduced. Therefore, the amplitudes of resonances and antiresonances are now wider and more likely to compensate each other. Since the centralized architecture introduces a larger shift of the resonance frequencies towards lower frequencies, this can lead to a slight increase in amplitude as the resonance and antiresonance frequencies (poles and zero respectively of equation (2) written in the presence of the HP protection architecture and R_b) are not precisely compensated. Further, it is interesting to evaluate the comparison of both architectures if the differential architecture was to be sized to present a capacitance C_e of 100 pF and the centralized sized to only present 10 pF. For that matter, the HF model of both HP protection architectures is used in simulations this time instead of the architectures themselves, with the previously mentioned values of C_e and with the PCB traces layout of Fig.9.

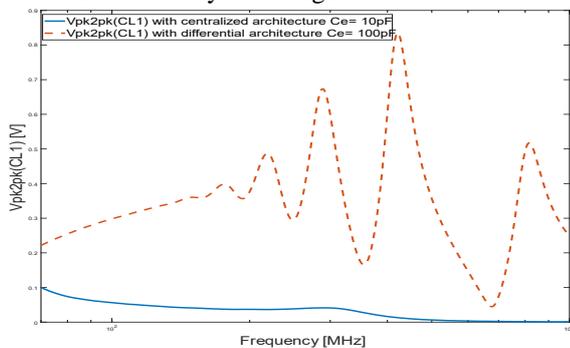


Fig. 14 Comparison between both the HP protection architectures in terms of injection levels onto C_{L1} with R_b and different architectures sizing.

As can be seen from Fig.14, the centralized architecture presents a considerably higher attenuation than the differential one in higher frequencies, with a much lower capacitance value. Therefore, the centralized architecture provides better filtering than the differential one and with a smaller capacitance value and thus a reduced size. In other words, the centralized architecture allows for a better capacitance value integration in the IC than the differential architecture. Finally, a certain tradeoff arises from this work; Sizing the diodes to have a larger area reduces its ON resistance, thus, improving the ability to diverge the HP inrush current. However, by doing so, the capacitive effect is reduced, thus, having a lower attenuation of the HF injection levels.

VI. CONCLUSION

Finally, this work has presented some predictive results when it comes to the design of PCB, external components, and HP protection architecture for optimal performance. Indeed, a tradeoff between external HP protection capacitor price and noise coupled onto the BMS IC is presented. Then, a ladder network theory-based approach is utilized to predict the maximum noise coupling frequencies. A comparison between two main HP protection architectures in terms of DPI injection levels is performed where the model was used to determine the resonances of interest and attenuation levels. Future work will focus on the use of a more realistic model of the impedance presented by the cell balancing switch to evaluate if the ladder network based analytical approach would still give an on-hand tool in the early design stages. Additionally, future work will also focus on the experimental validation of the presented models and reported tendencies.

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