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Integrating self-catalyzed InAs nanowires on Si(111) is an important step toward building vertical gate-all-around transistors. The CMOS compatibility and the nanowire aspect ratio are two crucial parameters to consider. In this work, we optimize the InAs nanowire morphology by changing the growth mode from Vapor-Solid to Vapor-Liquid-Solid in a CMOS compatible process. We study the key role of the Hydrogen surface preparation on nanowire growths and bound it to a change of the chemical potential and adatoms diffusion length on the substrate. We transfer the optimized process to patterned wafers and adapt both the surface preparation and the growth conditions. Once group III and V fluxes are balances, aspect ratio can be improved by increasing the system kinetics. Overall, we propose a method for large scale integration of CMOS compatible InAs nanowire on silicon and highlight the major role of kinetics on the growth mechanism.

1. Introduction

The successful growth of self-catalyzed III-V nanowires on Si(111)[1–7] has triggered a lot of interest in the nanoelectronics field since it allows integrating advantageous III-V properties on the Complementary Metal Oxide Semiconductor (CMOS) platform. New architectures such as vertically integrated 3D Gate-All-Around (GAA) transistors[8–10] are now present in the International Roadmap for Devices and Systems (IRDS). For this application, InAs[11–13] nanowires (NW) are the most interesting NMOS materials because of their high electron mobilities[14–16] and the possibility to grow them self-catalyzed on patterned Silicon wafer[17,18]. Moreover, high aspect ratios are reported in literature[19,20], which allows a good control of channel in the Field Effect Transistors (FET). Although a lot of studies focused on the aspect-ratio optimization of self-catalyzed nanowires integrated on silicon[21] or on the control of their crystalline structure[22], only a few studies consider the industrial requirements[23]. This is a crucial issue to move from fundamental studies to real applications.

In order to achieve CMOS compatibility, a few process milestones have to be achieved: (i) vertical nanowires should be integrated on Si(100) wafers, (ii) the growth should be self-catalyzed since gold creates mid-gap defects in Silicon, (iii) a high vertical yield should be achieved[1,11,24,25], (iv) the nanowire diameter should allow a low voltage pinch off of the FET channel[8] and finally (v) the whole process should not exceed the temperature of 450°C, which is the Back-End-of-Line (BEOL) thermal limit[26,27]. Thanks to recent technological advances, such as wafer bonding and Smart Cut technologies[28], the aforementioned mandatory growth on Si(001) substrates (i) is now relaxed since Si(111) wafer can be integrated on Si(001).

In this work, we report the CMOS compatible growth of InAs nanowires, at the wafer scale, on unpatterned Si(111) substrates by Molecular Beam Epitaxy (MBE). We first highlight the key role of surface preparation on the NW morphology (length, diameter and aspect ratio). Thanks to a robust statistical analysis of scanning electron microscopy (SEM) images, we demonstrate that the change from Vapor-Solid (VS) to Vapor-Liquid-Solid (VLS) growth mechanism improves the NW aspect ratio, which is fundamental for vertically integrated GAA-FETs. This is further confirmed by transmission electron microscopy (TEM) measurements. Finally, we present the growth of InAs NWs on patterned Si(111) substrates, which is a key building block for industrial applications.

2. Method

The experimental procedure we followed for this study can be divided in three main steps. First is the preparation of the substrate surface by chemical etching, degassing in an Hydrogen environment, and in-situ annealing with an Arsenic flux. Next is the nanowire growth in the MBE reactor. Finally, samples are characterized by SEM and TEM.

Before loading samples into the MBE system, two inches p-doped Si(111) wafers from Siltronix are wet etched with hydrofluoric acid (HF 5%) for one minute and rinsed in de-ionized water for another minute in order to remove the native oxide. Wafers are loaded immediately in our Riber 412 MBE system once dried with Nitrogen. Next, they are transferred into the MBE preparation chamber equipped with and Oxford Hydrogen (H_2) plasma cell. They are degassed at 200 °C for 1 hour under a H_2 gas or H_2 plasma flux. The gas flow is set to 1 sccm and the power used for the radio frequency cavity

of the Oxford cell is 250 watts. Samples are then transferred into the growth reactor and heated up to the growth temperature of 410 °C. Prior to growth, substrates are annealed at the growth temperature for 20 minutes under an Arsenic (As) flux of 2.0 x 10^{-5} Torr in order to create a (111)B surface on the non-polar Si(111) substrate[18]. Finally, the InAs NW growth is initiated by opening the Indium (In) shutter. The growth durations on unpatterned and patterned substrates are 1 hour and 20 minutes, respectively. It ends by closing the Indium shutter, and keeping the Arsenic flux on during the cooling down process (down to 200°C).

In the following, the adatom fluxes are 0.8 x 10^{-8}, 1.5 x 10^{-8} and 3.1 x 10^{-8} Torr for the Indium Knudsen cell and 1.2 x 10^{-5}, 1.8 x 10^{-5} and 2.4 x 10^{-5} Torr for the Arsenic cracker cell. An Indium flux of 3.1 x 10^{-8} Torr corresponds to a InAs growth rate of 0.02 monolayer per second on GaAs(001), whereas Arsenic is calibrated at 1 monolayer per second on GaAs(001) for a 2.4 x 10^{-5} Torr flux.

The nanowires are characterized by Scanning Electronic Microscopy (SEM, FEI Aztec-600i) using a 30° tilting angle, and an acceleration voltage ranging from 5kV to 30kV. The resolution is about 1nm for the 30kV acceleration voltage. The Transmission Electron Microscopy measurements are carried out in a JEOL J2100-FEG instrument equipped with a Field Emission Gun electron source. Analysis was performed at 200 kV accelerating voltage, at which the image resolution is 2.3 Å. The statistical analysis is carried out on SEM images considering at least 150 nanowires from each sample. Only vertical NWs are considered in the case of a patterned substrates.

3 Results and Discussion

3.1 InAs nanowires on Unpatterned Si(111) wafers

Figure 1 presents SEM images of InAs nanowires grown on Si(111) substrates having different surface preparations and identical growth conditions. This allows a direct comparison between both processes, H_2 gas (framed in green) and H_2 plasma (framed in red), for different V/III ratio and Kinetics. The Hydrogen surface preparation allows to keep the whole process CMOS compatible by reducing annealing temperatures as reported in [23]. First, it can be noticed that irrespectively of the surface treatment (gas or plasma) nanowires are fully vertical. This confirms the formation of a clean Si(111)B surface before nanowire growth. In addition, for higher In flux ($3.1x10^{-8}$ Torr), NWs on gas treated surfaces (**figure 1a** and **1c)** have better aspect ratio compared to their plasma counterparts (**figure 1b** and **1d).** This suggests that both surface treatments (gas and plasma), previously deemed equivalent, lead to different surface terminations. This behavior difference is even more visible when looking at the trends. Indeed, in the case of the gas preparation (**figures 1a,c,e,g**), the NW aspect ratio improves when increasing either the In or As fluxes. The exact opposite trend can be reported in the case of a plasma treated surface (**figures 1b,d,f,h**). This can be explained by different physical phenomenon such as adsorption, abstraction, etching [29] or passivation of the Si vacancies (VH_x) [30]. Each of them changing the surface chemical potential (μ), and thus the nucleation and growth conditions. This difference will be discussed further in the following.

In order to gain insight on the growth mechanisms on both surfaces, a complete statistical analysis of 18 samples has been carried out and is reported in **figures 2 and 3**. For each growth, several SEM images are taken all over the wafer, and an automatic procedure described in [23] measures both diameter and length of at least 150 NWs. Five families of comparable diameters (0-60 nm, 61-120 nm, 121-180 nm, 181-240 nm, 241-300 nm) are then built, and statistics are reported in **figures 2 and 3**.

First, the population of each family (in %) is reported in **figure 2** for different growth conditions and both surface preparations. It is defined as the ratio between the number of nanowires accumulated for one family to the total number of nanowires (at least 150) considered for that sample. Interestingly, when the Indium flux is low (bottom line in **figure 2**), no differences prevail between gas and plasma treated surfaces and the majority of the wires have a diameter above 100 nm. On the opposite, the difference observed in **figure 1** is striking for an Indium flux of 3.1 x 10^{-8} Torr (first line in **figure 2**). In that case, NW diameters on gas treated surfaces are smaller compared to the plasma ones and the 0-60 nm population is majoritarian for highest Indium and Arsenic fluxes (**1st row and 3rd column in figure 2**). Considering the electrostatic control of a FET gate, this difference is crucial for future devices and could be explained by a different landscape of the chemical potential on both surfaces as proposed in the following.

In **figure 3**, the mean NW length (in nm) for each population is reported for both surface preparations (gas and plasma) as a function of the growth conditions (In and As fluxes). For low Indium fluxes (**2nd and 3rd rows in figure 3**), irrespectively of the surface treatment, the mean NW length is comparable in each family, and increases with the NW diameter. This trend is commonly observed in literature for NW growth[1,24]. When the Indium flux is higher (**1st row in figure 3**), a difference appears between the two surface preparations when increasing the Arsenic flux. In the extreme case (highest In and As fluxes; **1st row and 3rd column in figure 3**), which corresponds to nanowires in **figure 1c,** the highest aspect ratio is achieved for the gas prepared surface. Here, the nanowire length does not increase anymore with its diameter. This unexpected behavior was recently reported for InP nanowires by Gao et al.[31] and was attributed to a change of the growth mechanism from Vapor-Solid (VS) to Vapor-

Liquid-Solid (VLS). This change of growth mode is directly correlated to the system kinetics and to the diffusion length of adatoms on the substrate surface. In the case of a gas treated surface, the distribution of the surface chemical potential ($\Delta\mu$) before growth is close to zero, allowing large diffusion length (l_g) of adatoms on the substrate surface. In that case, increasing the system kinetics will provide more materials for NW growth, which leads to a switch from a VS to a VLS growth mode. A direct consequence is an improvement of the NW aspect ratio. On contrary, the surface chemical potential, after a plasma process, should exhibit large variations, which traps adatoms in local minima of μ and reduces l_g. In that later case, increasing the system kinetics leads to the accumulation of more adatoms in local minima of μ, which kills the vertical growth rate (shorter NWs). This change of growth mode is a key enabler for developing new GAA devices.

Finally, High-Resolution (HR) TEM measurements are carried out to probe the shape of the nanowire tips. This structural and morphological investigation is reported in **figure 4**. In the case of non-optimized growth (low kinetics, **figures 1e,f**), the NW tip is flat (**figures 4c,d**, respectively) regardless of the surface preparation. As reported in literature [32], this is typical of a VS growth mode. On contrary, the NW tips present a round shape for the highest kinetics, as shown in **figures 4a,b** (corresponding to a NW grown in **figure 1c**). This is characteristic of a liquid droplet crystallization [33] during the cooling down of the samples. A complete TEM study, based on several images taken at different viewing angles (**figure SI-1**), confirms this observation. This indicates a VLS growth mode of the InAs NWs and the presence of an Indium droplet that crystallizes into InAs during the cooling down process. Interestingly, the chemical potential of the Indium droplet surface appears to be lower that of the InAs (111) one, since the NW vertical growth rate increases drastically for small diameters.

Consequently, considering the SEM images (**figure 1**), the statistical analysis (**figure 2 & 3**) and finally the TEM inspection (**figure 4**), while focusing on the particular sample in **figure 1c**, we can conclude that the InAs nanowire growth mode changes from VS to VLS when the overall growth kinetics increases.

3.2 InAs nanowires on patterned Si(111) wafers

Now that the nanowire aspect ratio is optimized on unpatterned substrates, our goal is to transfer this process to patterned Si(111) wafers. **Figure SI-2** details the patterning steps of the Si(111) substrates and how holes arrays are obtained having diameters of 120, 150 and 200 nm and pitches of 100, 250 and 500 nm. Unfortunately, a direct transposition of our processes to patterned substrates leads to a low yield of nucleating NWs as reported in **figure SI-3**. This can originate either from the patterning steps, changing the Si(111) surface termination, or from the presence of SiO_2, changing the adatom diffusion length on the substrate surface. Both the surface preparation and the growth conditions have thus to be adapted in order to improve the yield of vertical NWs.

In the following, a pre-growth annealing at 650°C for 20 min under an Arsenic flux of 2.0×10^{-5} Torr is added to the process flow in order to improve nucleation. This is known to promote the formation of a Si(111)B surface[18], and thus the growth of vertical NWs. **Figure SI-4** presents InAs NWs grown with these conditions and the better vertical yield observed in the case of plasma treated substrate. This difference with growths on unpatterned wafers can originate from the surface chemical potential of the SiO_2 layer being less affected by the H_2 plasma than the Si(111) one; and from a better removal of resist residues (due to patterning) by H_2 plasma[34]. All these

observations lead us to only consider the plasma preparation for growth in patterned substrates. An example of InAs NW grown with this surface preparation is reported in **figure 5**. High vertical yield, high aspect ratio and absence of parasitic growth are confirmed by these SEM images.

A statistical analysis of the NW morphology as a function of growth conditions and patterning parameters is reported in **figure 6**. For each pitch, the vertical yield (**1st row**), the mean diameter (**2nd row**) and the mean length (**3rd row**) of InAs nanowires are reported for each growth condition. Each nanowire array is characterized by SEM and analyzed separately. The yield corresponds to the ratio between vertical nanowires and total number of holes in an array. Mean length and mean diameter are calculated only on the fully vertical NWs.

First, it can be noticed that the vertical yield is pitch independent and increases with the hole diameters. This is in good agreements with observations from literature concerning self-catalyzed InAs NWs[24]. It is above 60% in most of the cases and globally decreases when reducing the hole diameter. A maximal yield of 90% is reached for the lowest V/III ratio (in blue), indicating the key role of Indium in the InAs NW nucleation. Moreover, both the NW diameter and length are marginally affected by the hole diameter and the pitch. This indicates a low competition between wires in the patterns to collect Indium and Arsenic adatoms. Since group V elements have a very low sticking coefficient (<<1) compared to group III ones (~1)[35], only Indium adatoms are expected to diffuse on the substrate surface. This allows us to estimate an Indium diffusion length (l_g) close to the hole diameter in our patterns and almost no diffusion on the SiO_2 layer. Finally, the evolution of the NW length and diameter as a function of both the Indium and Arsenic fluxes allows to optimize the NW aspect ratio. If we first consider the lowest fluxes (in green), increasing either the Indium flux (in blue) or the

Arsenic one (in brown) do not change the NW length and only marginally the NW diameter. On the contrary, increasing both at the same time (in purple) roughly doubles the length without noticeable influence on the diameter. This indicates that the “green” growth conditions provide a good balance to the system: the growth is neither group III or group V limited. When increasing only one flux, the balance is broken and the NW growth becomes either group III (in brown) or group V (in blue) limited. Doubling both fluxes at the same time, not only keeps the system balance, but also increases its kinetics: the length is doubled while the diameter remains constant (in a first approximation), which results in a doubled NW aspect ratio. This clearly indicates how to optimize the nanowire geometry for the next generation of vertically integrated GAA-FETs: first balance group III and V fluxes as a function of the patterns, and then increase the system kinetics to improve the NW aspect ratio.

4 Conclusion

In this paper, we investigate the growth of InAs nanowires on Si(111) substrates by MBE using different surface preparations. We show how growth kinetics (In and As fluxes) and surface treatments (H_2 gas or plasma) influence the nanowires morphology (length, diameter and aspect ratio). A statistical analysis of SEM images and HR-TEM measurements confirm a change of growth mode from VS to VLS when increasing the system kinetics. A direct consequence is a large improvement of the NW aspect ratio, which is promising for building vertically integrated GAA-FETs. A direct transfer of this process onto Si(111) patterned substrate result in a degraded nanowire morphology. This is explained by different chemical potential, and thus different diffusion length, on both substrates. When adapted, the surface preparation allows to reach vertical yields

above 80% regardless of the NW density. Once the group III and V fluxes are balanced, the system kinetics can be increased in order to improve the aspect ratios. This approach allows to optimize the InAs NW integration on Silicon for efficient channel control in vertically integrated GAA-FETs.

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AUTHOR CONTRIBUTION:

D.S.D. and S.R.P. conceived the project, experiments, grew the samples and performed SEM measurements.
P.-F.F. and F.C. measured the nanowires by TEM.
N.M. and G.L. prepared the patterned substrates.
D.S.D., F.C. and S.R.P. analyzed the measurements and wrote the manuscript with input from all the authors.

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Additional information:

The authors declare no competing financial interests.

Figure

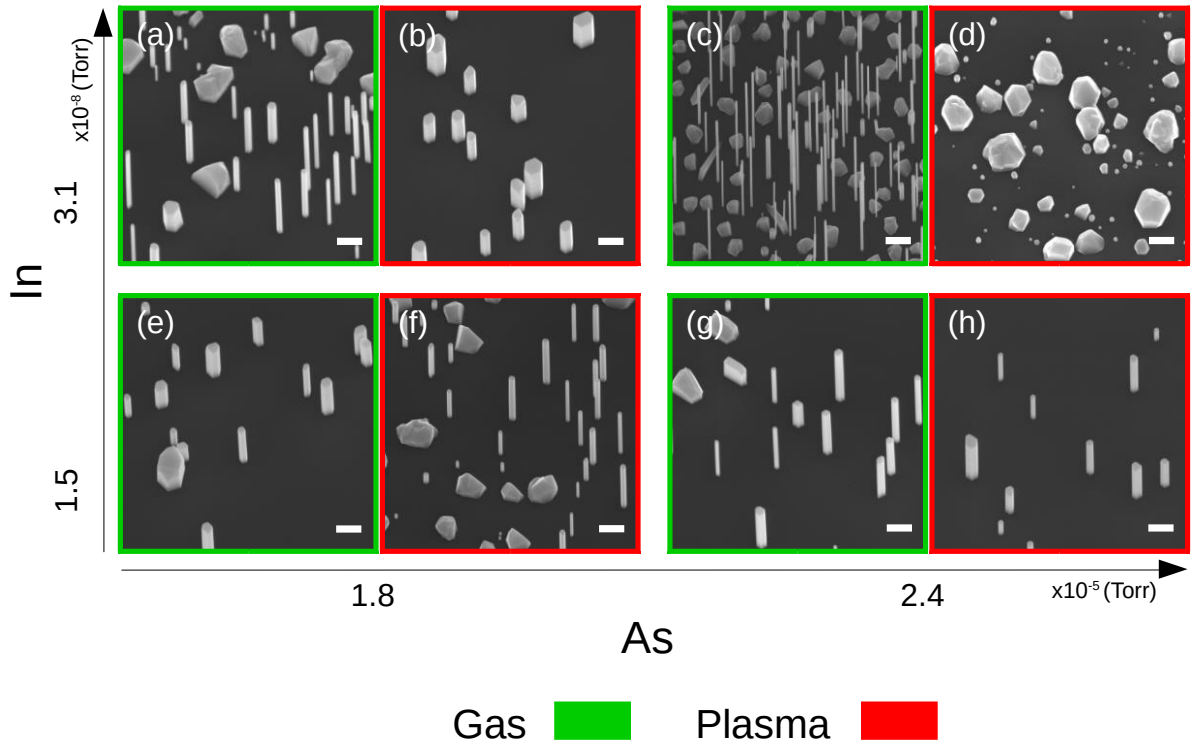

Figure 1. Evolution of InAs nanowire morphology as a function of growth conditions and surface preparation. The In flux increases from bottom to top and the As one from left to right. The green framed SEM images (**a,c,e,g**) correspond to a H_2 gas surface preparation whereas it is a plasma one for the red frames (**b,d,f,h**). The scale bar is 500 nm.

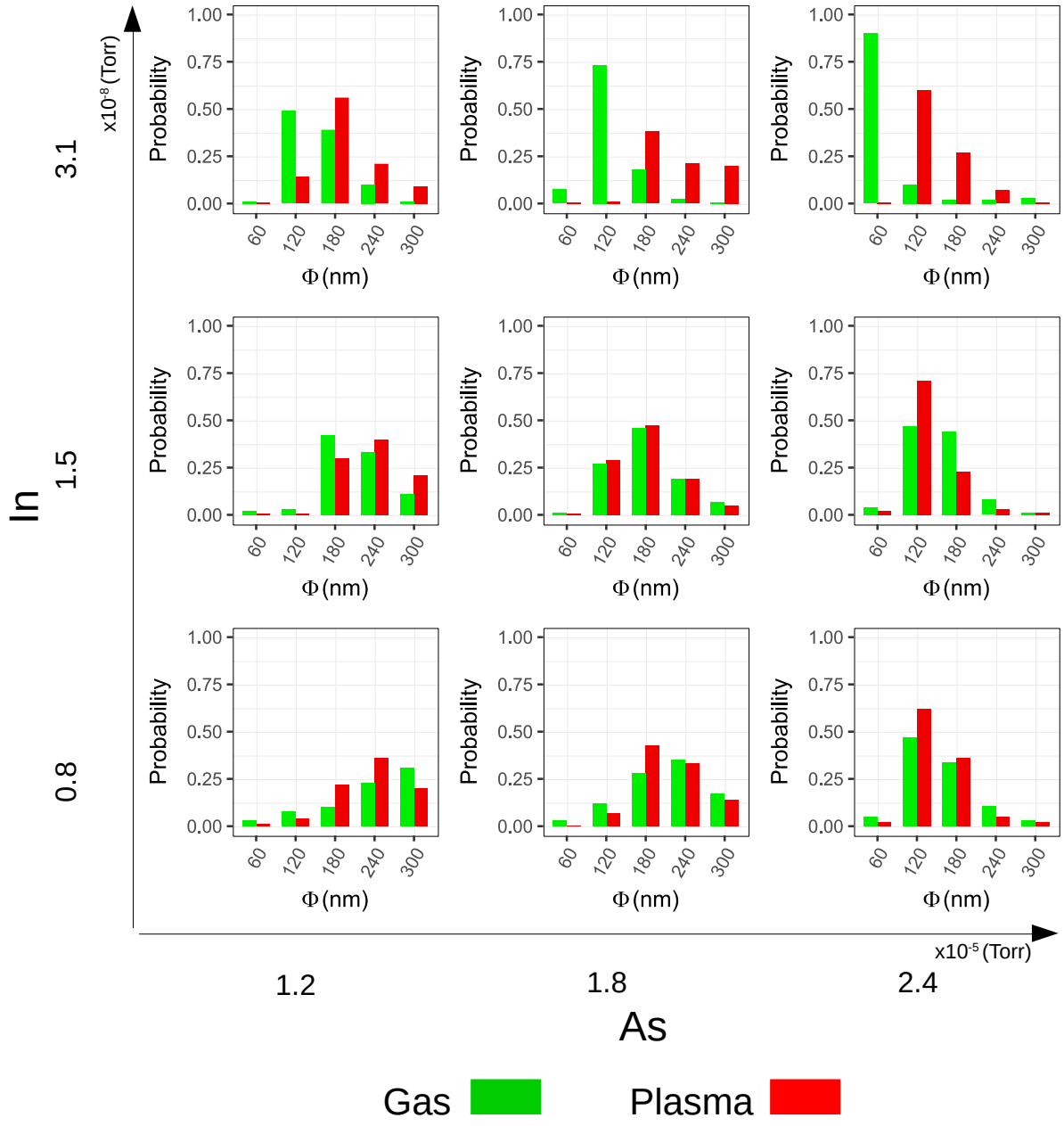

Figure 2. Impact of the H_2-gas (in green) and H_2-plasma (in red) surface preparations on the nanowire diameter. Each of the 9 scatter plots correspond to different growth conditions (In and As fluxes reported on left and bottom, respectively). For each plot, the x-axis corresponds to the diameter (in nm) and the y-axis to the population (in %) of the corresponding nanowire family. Green boxes correspond to a H_2 gas preparation, whereas it is H_2 plasma for the red ones.

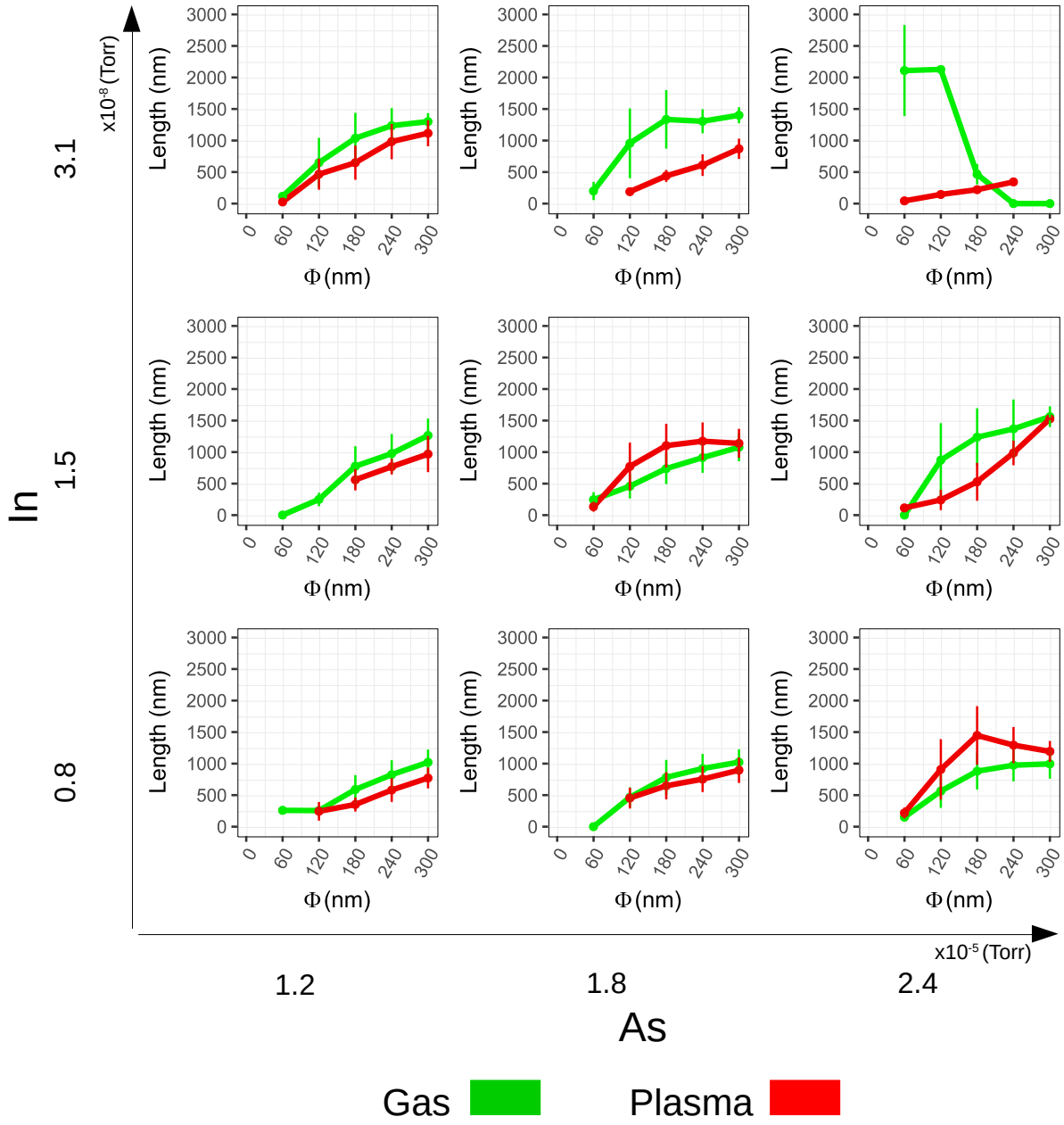

Figure 3. Impact of the H_2-gas (in green) and H_2-plasma (in red) surface preparations on the nanowire length. Each of the 9 scatter plots correspond to different growth conditions (In and As fluxes reported on left and bottom, respectively). For each plot, the x-axis corresponds to the diameter (in nm) and the y-axis to the length (in nm) of the corresponding nanowire family. Green lines correspond to a H_2 gas preparation, whereas it is H_2 plasma for the red ones.

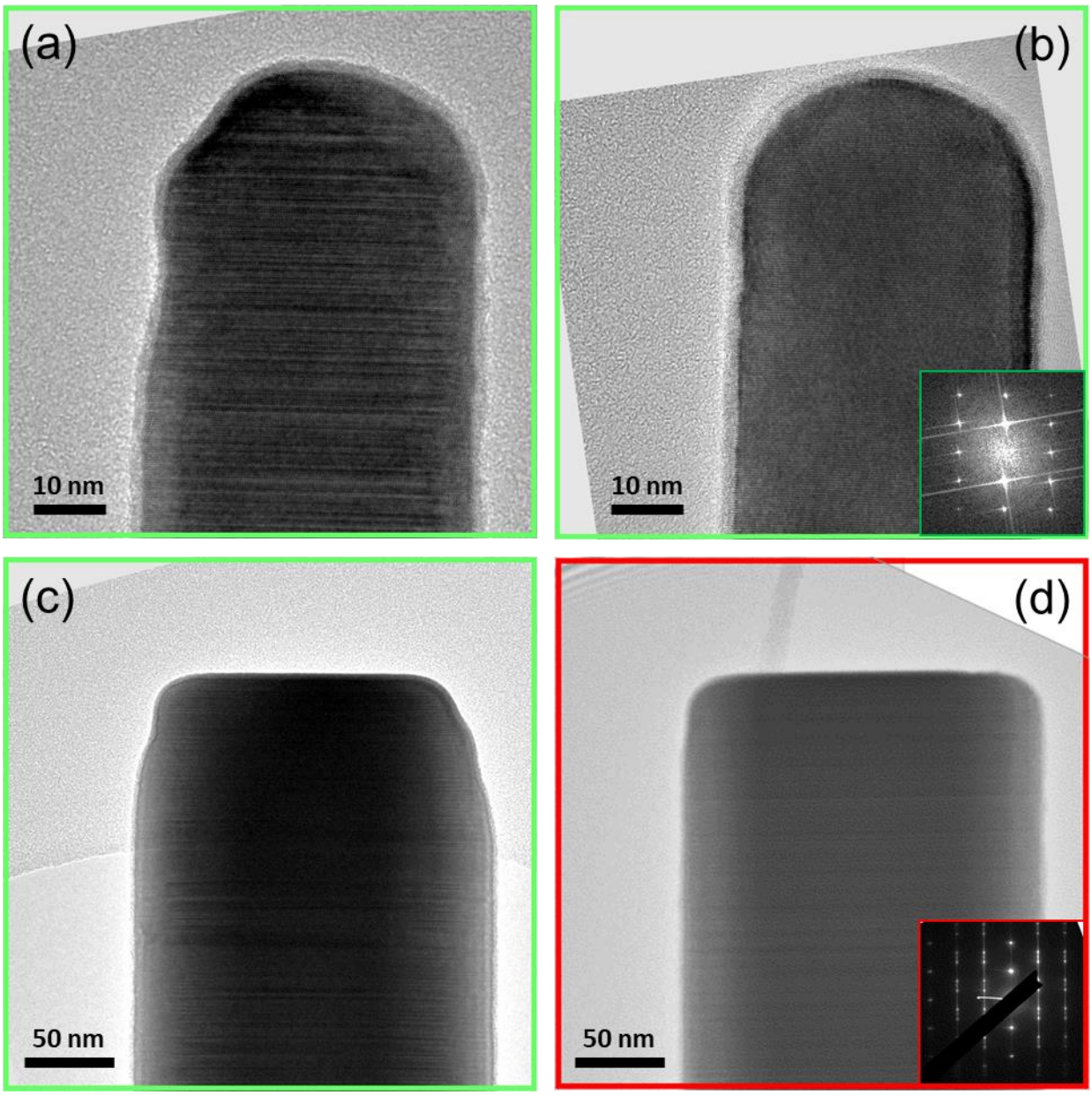

Figure 4. Flat and rounded shapes of the InAs nanowire tips viewed by HR-TEM. **(a), (b)** correspond to an InAs nanowire from **figure 1c. (c), (d)** correspond to **figure 1e,f**, respectively**. (a), (c)** and **(d)** are viewed along the [110] direction, while **(b)** is viewed along the [112] direction (rotation of 30°). The growth direction is <111> in all the cases.

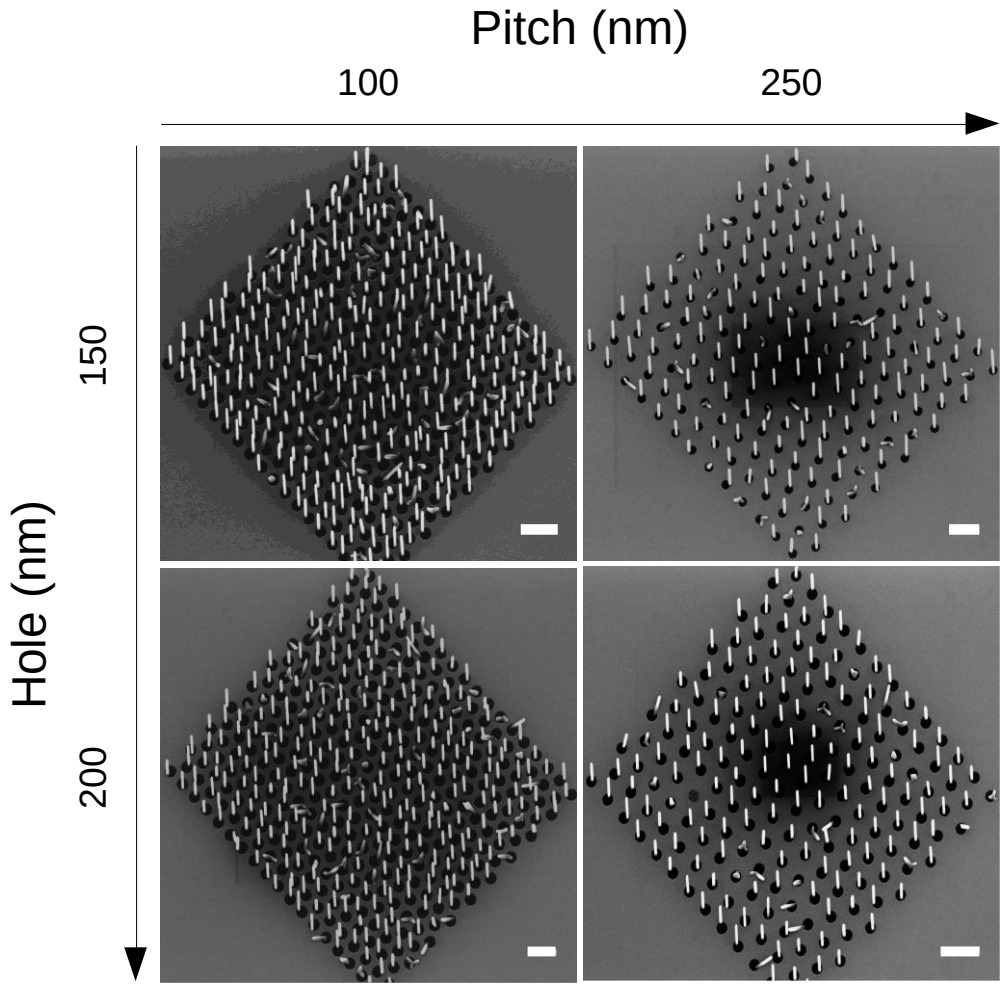

Figure 5. SEM images of InAs nanowires grown on patterned substrates. The pitch increases from left to right and the hole diameter from top to bottom. The Indium flux is 6.2 x 10^{-8} Torr and the Arsenic one is 0.6 x 10^{-5} Torr. Scale bars are 500 nm.

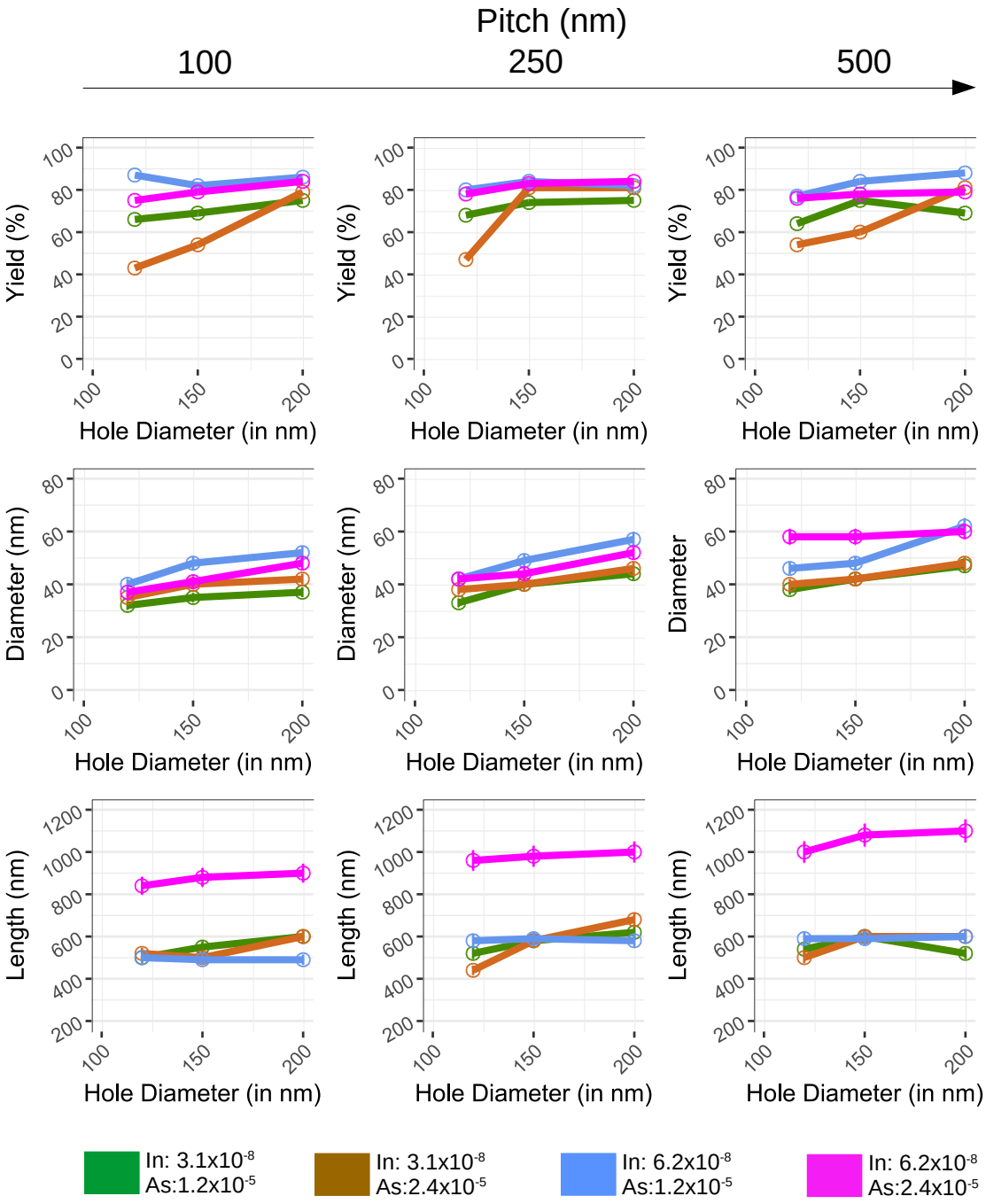

Figure 6. Statistical analysis of the InAs nanowire grown on patterned Si(111) wafers. Each color corresponds to a specific set of growth conditions: (i.e. a specific In and As flux). For each plot, the x-axis corresponds to the pattern hole diameters (in nm). The y-axis represents the vertical yield (in %) for the 1st line, the mean diameter (in nm) for the 2nd line and the mean length (in nm) for the 3rd line. Each column corresponds to a different pitch: 100, 250 and 500 nm.

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