New Measurement Method to Investigated Service Life of Protection Networks exposed to ESD

François Ruffat, Fabrice Caignet, Alexandre Boyer, Fabien Escudie, Guillaume Mejecaze, Frédéric Puybaret

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F. Ruffat[a,*], F. Caignet[a], A. Boyer[a], F. Escudié[b], G. Mejecaze[b], F. Puybaret[b]

[a] *LAAS-CNRS, University of Toulouse, Toulouse, France*
[b] *CEA, DAM, CEA-Gramat, F-46500 Gramat, France*

Abstract

This paper presents a new measurement method that enables investigating the degradations of protection networks under cumulative ESD pulses. The setup is based on a Transmission Line Pulse (TLP) combined with Time Domain Reflectometry (TDR) to get access to the complex impedance of the device under test. One of the advantages of the technique is that the frequency behaviour of the DUT is extracted as the same time the device is aged. The method is validated on a stable component and different devices are tested. Results show that after a certain number of pulses, the characteristic of the device have changed significantly. The extracted impedances can then be used into system design flow to investigate the impact of ESD stresses on sustainability of ESD protection network. Observations on the deviations of these input protection networks could also have impact on the electromagnetic immunity networks.

1. Introduction

Depending on the mission profile, embedded electronic products must survive harsh environments for periods ranging from a few months to several years. In such environments, Electrical Fast Transient (EFT) such as ElectroStatic Discharge (ESD) may have a significant occurrence. As an example, each automotive electronic product has to survive more than ten thousand stresses during its entire life (10 years) [1]. The Industry Council on ESD Target Levels exposes some system level ESD problems in [2]. Based on this assessment, standards to certify the system level to ESD stress have been created, the most common is the IEC 61000-4-2 [3] or the more recently the HMM that directly stress Printed Circuit Boards (PCB) [4].

According to the safety requirements, a set of protections is implemented into Printed Circuit Board (PCB) to prevent Integrated Circuits (IC) from any malfunctions [2]. For system pins exposed to external stresses, passive components such as resistors, capacitors or inductors, dedicated protections such as Transient Voltage Suppressor (TVS) or even on-chip protections can be used. The protection network is built during the design phase of the system, but no investigations is performed to ensure that its characteristics will remain the same after years, and so to know the deviation that could appear after a large number of EFT events. In order to study the degradation of protection devices to ESD, the Transmission Line Pulse (TLP) generator [5] is a valuable tool to produce representative and reproductible pulses with similar characteristics than ESD. This equipment was used as stress source in [6] and [7] to investigate drift of thick film resistors according to pulse duration and amplitude. The static I(V) characteristics are extracted during stress. In [8], a Q(V) model has been produced in order to study the ESD-induced degradation of ceramic capacitor. The derivative of the Q(V) curve is the value of the capacitance for each voltage. Under linear regime assumption, the capacitance value can be estimated with this technique. Even if this approach is sufficient to measure the resistance or capacitance shift, the impact on complex impedance remains unknown. [9] exposes two techniques, based on TLP measurement, to model the capacitance variation due to capacitor bias. It permits to model the transient response of a capacitor to ESD discharge without any frequency measurement. But the evolution of complex impedance was not given. Some interesting information, such as the Equivalent Serial Resistance (ESR) or the parasitic inductance due to the package influence, was not determined. Another measurement technique based on Vector Network Analyser (VNA), requires tedious handling of the tested devices [10]. Even more if we want to investigate the effect of

* Corresponding author. fruffat@laas.fr

cumulative ESD stresses on devices.

In this paper, we propose a new measurement method to stress component with cumulative pulses and check any deviation of the device characteristics at the same time (without any kind of handling on the setup). The stress and measurement methods are built around a TLP generator combined with a Time Domain Reflectometry (TDR) to get the frequency characteristic of the Device Under Test (DUT). The fundamentals are described in papers [11] and [12].

The whole setup as well as the measurement technique and computation to obtain the frequency behaviour of the DUT is presented in Section II. In the third Section, the stress method to accelerate aging is presented. In the fourth Section, two cases of degradations are presented, one considering a resistor, the other a capacitor. The main deviations of the parameters of the devices are extracted from its complex impedance. Regarding this first results, it is clear that protection networks will be considerably modified. The last paragraph is dedicated to conclusion.

2. Presentation of the TLP-based TDR measurement method

The aim of this method is to obtain a characterization in frequency domain of a two-terminals protection device (e.g. filtering capacitor, TVS) based on the extraction of the reflection coefficient measurement of a load impedance through a TDR method [11].

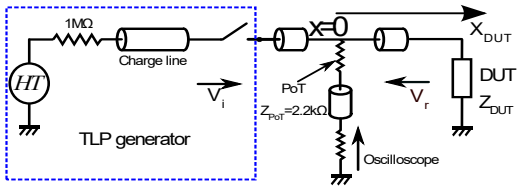

Fig. 1. Schema of TLP-based TDR measurement method

The TLP-based TDR method principle, reported in Fig. 1. is based on the injection of a forward voltage V_i, which is reflected as V_r, in the load impedance Z_{DUT}. V_i and V_r measurements allow to compute the frequency impedance, where Z_0 is the characteristic impedance of the cable that conducts V_i. More details and a validation can be found in [11].

The pulse is generated by a TLP generator (HPPI TLP8010C model). It generates a 100 ns long pulse with a rise time of 100 ps and a maximum voltage of 4 kV and current of 80 A. A Pick-off Tee (PoT) linked to an oscilloscope (Tektronix DPO71254C, 100 GS/s BW=12 GHz) is used to measure the voltage on one point of the line (x = 0). All the lines between the different elements are 50 Ω adapted. The measured voltage V_m at a given distance x is defined by (1) and is the superposition of V_i and V_r.

$$V_m(x,t) = V_i(x,t) + V_r(x,t) \quad (1)$$

From the measurement of V_m, V_i and V_r have to be separated to compute the reflection coefficient given by (2). A calibration method is needed to extract V_i independently of the connected load, at the output of the TDR. A matched load Z_0 is used instead of Z_{DUT} to cancel V_r and ensure that $V_m = V_i$. The setup parameters and the charge voltage level of the TLP are the same than those used to measure V_m on Z_{DUT}.

As shown in (1), V_i and V_r are separated to obtain a measurement of the impedance. The TDR gives either the transient reflection coefficient or the impedance of the DUT. V_i and V_r spectra are computed by a Fourier transform in order to obtain the reflection coefficient or the S_{11}-parameter in frequency domain (2).

$$S_{11}(x_{DUT},f) = \frac{Z_{DUT}(f) - Z_0}{Z_{DUT}(f) + Z_0} = \frac{V_r(x_{DUT},f)}{V_i(x_{DUT},f)} \quad (2)$$

The S_{11}-parameter is obtained after a dedicated calibration setup detailed in [11]. In order to validate the measurement approach, the impedance of a 1 nF C0G capacitor is measured either with a VNA (reference measurement) and the TLP-based TDR method. Fig. 2 compares the modulus of the impedance of the capacitor measured either with the VNA or the TLP under 100 V pulse injection. The TLP-based TDR measurement fits very well with VNA measurement. Between 10 MHz and 1 GHz, the gap is under 1%. The resonance peak is well represented, as well as the ESR of 40 mΩ.

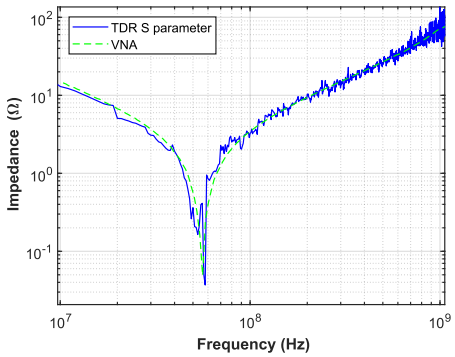

Fig. 2. Comparison between VNA and TLP-based TDR (100 V) measurements on the 1 nF C0G capacitor

3. Presentation of the stress method based on TLP

The main purpose of TLP is to generate transient pulse representative of ESD in a reproductible manner. It can also be used to mimic electrical stress due to ESD events encountered by an electronic equipment during its service life. In this paper, the TLP is used both to accelerate the degradation of the DUT and recharacterize its impedance at any time

without the need to change the measurement system. Thus, the derating of the DUT according to the number of received pulses is performed and measured.

The following two-fold procedure is used: first a series of pulses with linearly-increasing amplitude is sent up to the destruction of the DUT in order to determine its breakdown level. Moreover, as its impedance may change with the applied voltage, it is fundamental to determine the voltage range on which the DUT behaves linearly. After each pulse, the impedance is computed according to the method described in Section 2, to determine the voltage range of the linear regime.

Secondly, to obtain the degradation characteristics of the components, a succession of stress pulses and measurement pulses is operated. The flow of this technique is presented in Fig.3. The amplitude of the stress pulses is chosen such as it does not exceed the breakdown level. The amplitude of the measurement pulses falls within the voltage range of the linear regime.

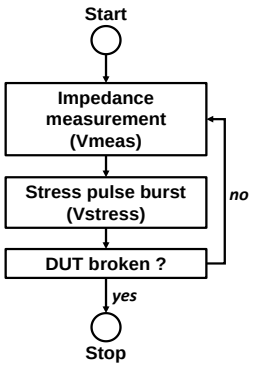

Fig. 3. Flowgraph of the stress-measurement-stress procedure

The stress consists in a succession of N-pulses at V_{stress} voltage level followed by one pulse with an amplitude of $V_{measurement}$ to measure the DUT impedance, as shown in Fig. 4. V_{stress} and N-pulses are given for each test. $V_{measurement}$ is fixed at 50 V. The duration between two successive stress pulses Δt is defined by the type of breakdown (voltage limit or energy limit). To verify the relevance of the obtained results, the tests are repeated on some samples.

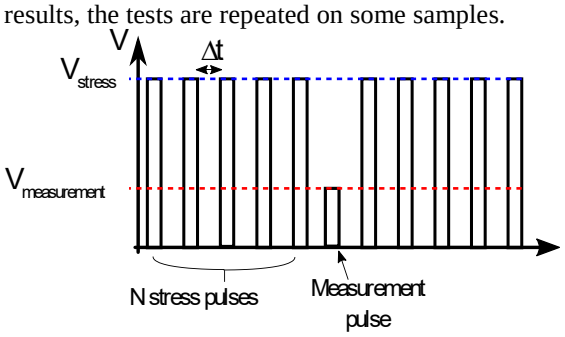

Fig. 4. Sequence of stress and measurement pulses

Impedances are obtained for each component. The log-log least squares method is used to get the characteristic parameters of the components.

4. Experimental results of ESD stress

The components used for these experiments are specified in Table I. They are common devices that can be used to protect system input against EFT or even electromagnetic disturbances. All these devices are mounted in 0805 cases.

TABLE I. TESTED COMPONENT SPECIFICATIONS

Component	Reference	Specification
50 Ω thin-film resistor	Panasonic ERA6AEB49R9V	R=49.9 Ω, Pmax=0.125 W tolerance 0.1% Vbreakdown = 800 V
X7R capacitor	Kyocera avx 08055C102KAT2A	C=1 nF, VDCmax=50 V tolerance 10% Vbreakdown = 940 V
Multilayer ferrite inductor	Murata LQM21PN1R0MC0D	L=1 µH Isat=0.8 A tolerance 20% V or I breakdown not seen

These three different components are chosen because of their three different breakdown mechanism. A preliminary study of their breakdown mechanism is made. The 50 Ω resistor is destroyed by the energy. The TLP duration has an influence on the breakdown voltage. A correlation between duration and breakdown voltage is clearly seen for three different pulses duration (50 ns, 100 ns and 500 ns). The X7R capacitor is broken due to the overvoltage. With a similar protocol as the 50 Ω resistor, the X7R is broken at a same voltage, regardless of the pulse duration. An inductor is also tested. This component is not broken during the test. The type of breakdown influences the configuration of the delay between two pulses to prevent the overheating of resistor due to the thermal dissipation of the ESD pulse energy. This overheating will accelerate thermal aging of the resistor, which is not covered by this study. A computation of temperature increase is realized for the resistor based on the device datasheet. A duration of 2 s has been chosen as the internal temperature increase is less than 0.03 K, and it limits the whole duration of the experiment.

4.1. Experimental results of the resistor degradation

Fig. 5 reports the variation of the nominal value of the resistor after a number of pulses from 300 V to

500 V TLP. For an impedance higher than 51 Ω (i.e. a variation larger than 2% of the nominal value), the component is considered to be degraded. At 300 V, no components are degraded up to 1000 pulses. At 400 V, all the resistors are destroyed, showing a large increase of the resistance value. At 500 V, the degradation characteristics are the same than those for 400 V.

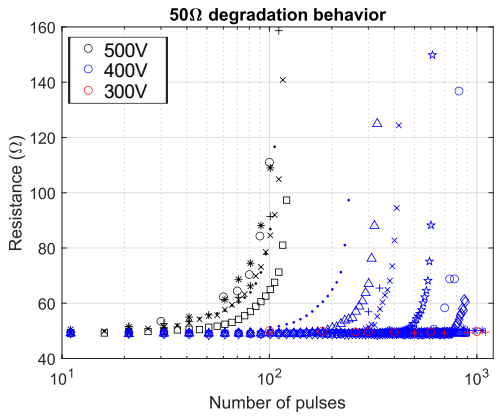

Fig. 5. 50 Ω resistance degradation according to the number of TLP stress from 300 V to 500 V

For 400 V characteristic, the number of pulses required to degrade the component is not clearly seen in the graph. A statistical approach to determine this number is essential.

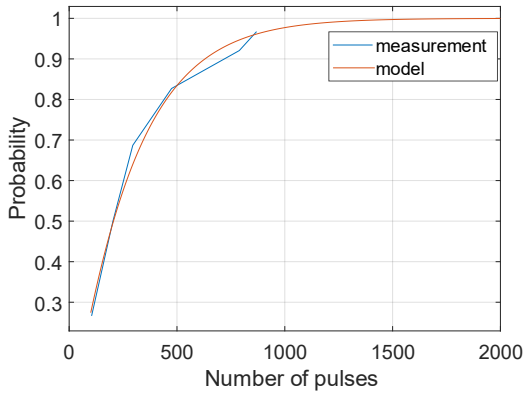

Fig. 6. Comparison measurement probability of degradation vs model

In Fig. 6 the failure probability according to the number of pulses is presented. A Weibulll law fits the experimental data curve. The fiting model (3) parameter are β = 1.07 and γ = 289.20. The probability of a degradation of 50% of the components is obtained for 200 pulses.

$$P = 1 - \exp\left(\left(\frac{N}{\gamma}\right)^{\beta}\right) \qquad (3)$$

At 500 V a clear degradation is observed for the 5 tested components. The number of pulses to increase the resistance above 51 Ω is about 40 pulses. It can be noticed that before the destruction of the resistance, its value could increase up to 150 Ω.

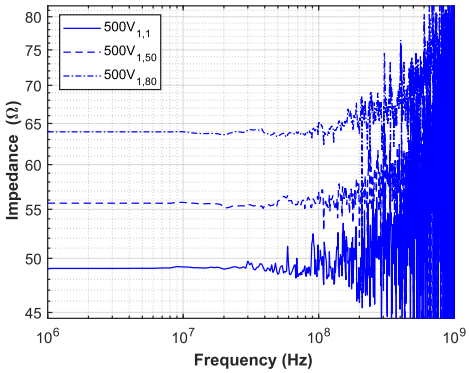

Fig. 7. Z(f) of the 50 Ω resistance (component 5) before and after stress

Fig. 7 presents the impedance of the resistor before and after stress, respectively after 1, 50 and 80 500 V-pulses. The variation of the impedance is clearly seen.

4.2. Experimental results of the capacitor degradation

Fig. 8 presents the evolution of the complex impedance of the X7R capacitor after 1, 1100 and 1400 ESD pulses. All curves show an obvious evolution of the impedance due to the ESD pulses. The value of the capacitance strongly decreases. The ESR is also decreases (0.5 Ω, 0.3 Ω, 0.1 Ω). The parasitic inductance value does not vary. The inductance is due to the package of the component. This curve permits to measure the capacitance value. But an automation of the ESR measurement is too complex for our purpose.

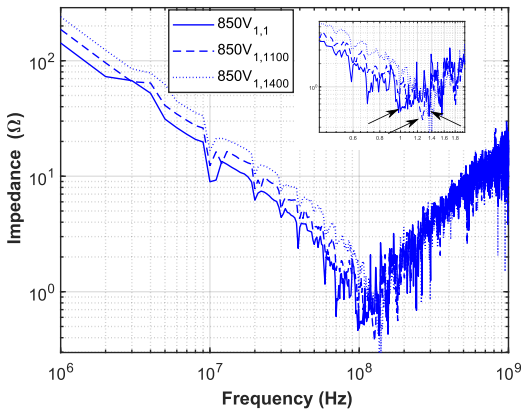

Fig. 8. Complex impedance of the X7R capacitor after

different numbers of pulses

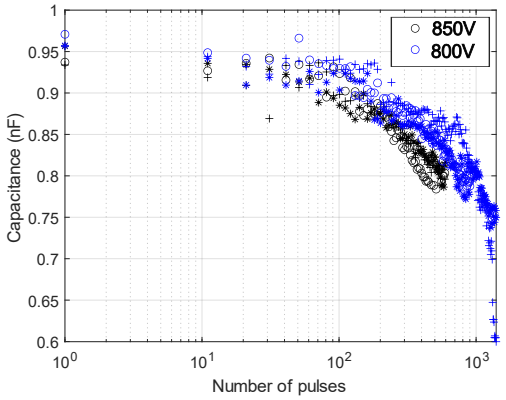

Fig. 9. X7R capacitor degradation according to the number of TLP stresses from 800 V to 850 V

In Fig. 9, a 1 nF X7R capacitor is investigated. The variation of the capacitance for two devices is reported, depending on the number of pulses at respectively 800 V and 850 V closed to the breakdown voltage (940 V). The two different aging behaviours are similar but the degradation arises for a smaller number of stress with 850 V stress. For 850 V stress, the failure is reached after 500 pulses and after more than 800 pulses for 800 V stress. The device always behaves as a capacitor. This is clearly shown in Fig. 8 where the impedance of the capacitance after 1, 1100 and 1400 pulses is reported.

4.3. Experimental results of the inductor degradation

The last type of tested component is the inductor. This component is stressed with 2000 V pulses. The frequency response is reported in Fig. 10 before and after 1000 pulses.

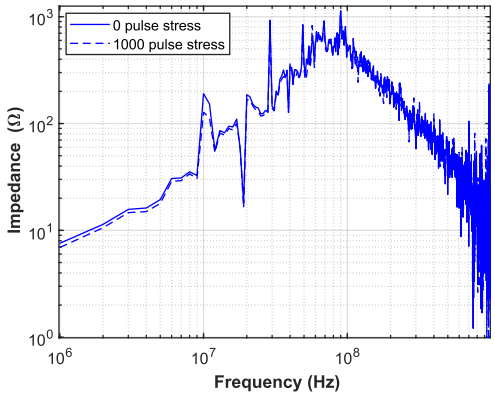

Fig. 10. Z(f) of multilayer ferrite inductor after different number of pulses

The two curves are identical. The inductance value is 0.85 µH. Parasitic capacitance could be obtained too at 4,0 pF. This component exhibits no degradation due to cumulative stresses, proving the high robustness of this component to ESD stresses.

5. Conclusion

In this paper, we propose a TLP-based TDR method that permits both to study the impact of cumulative stresses on devices and, at the same time, to get access to the characteristics of the components in order to follow gradual degradation. The measurement of S-parameters at higher voltages than VNA measurements is obtained and thereby the complex impedance of devices. The obtained frequency models can be used in design flow to estimate how the efficiency of ESD protection networks could be modified by multiple stresses during system service life. A precise analysis of degradation behavior for 50 Ω resistor, X7R capacitor and chip inductor has been conducted. For example, the complex impedance of the X7R capacitor is significantly modified. Its use in a protection network could change the long-term protection efficiency to ESD or could have a consequent impact on electromagnetic immunity.

In this paper, a classic TLP waveform is used. Thanks to the TLP-based TDR method, it is henceforth possible to stress devices with other pulse waveforms such as Human Metal Model (HMM)-to study the degradation behavior of the components for other kinds of stresses.

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