A New 77 GHz Sampling Mixer in 28-nm FD-SOI CMOS Technology for Automotive Radar application

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***Abstract*—This paper presents a low-IF sampling mixer topology based on a new pulse shaper and designed for automotive radar application. The sampling mixer operation principle is described. Then an original pulse shaper topology convenient for a 77 GHz sampling operation is proposed and implemented in 28-nm FD-SOI CMOS technology. Measurement results show a 1dB input-referred compression power (ICP1dB) of +6.7 dBm and a 9.1 dB Noise Figure (NF) with a conversion gain of -0.7 dB. The power consumption of the mixer is 10 mW on a 1V supply.**

***Keywords*—Millimeter-wave, passive mixer, receiver, Low duty cycle, W band.**

I. INTRODUCTION

The growing concern about driving safety is challenging the automotive industry with the need of very efficient radar sensors. Using mm-wave frequencies allows a good range resolution with a better circuit integration but is also a challenge for circuit designers who must fulfill stringent requirements especially on the receiver front-end.

The main challenge is the trade-off between noise and linearity. An automotive radar must cope with multiple signal reflections that desensitize the receiver if the linearity is not high enough. At the same time, the noise level limits the detection of distant targets by the receiver.

Recently, the scaling down of CMOS processes coming with the increase of f_t makes CMOS a good substitute to BiCMOS processes for 77 GHz applications, especially when cost target requires single chip solutions.

The literature related to CMOS radar receivers highlights that high performances are reached with passive mixers that provides high linearity and zero DC power consumption [1]. Consequently, a passive mixer has been chosen for the presented radar front-end. Nevertheless, passive mixers suffer from low conversion gain that affect the receiver NF. Better performances can be reached by using a passive sampling mixer that still benefits from good linearity while improving the conversion gain [2].

Requirement for a low duty cycle Local Oscillator (LO) signal appears as a roadblock at 77 GHz. From this observation, the integration of a passive sampling mixer based on a new pulse shaper to generate a pulsed LO signal is proposed in this paper.

The sampling mixer principle is presented in section II. Section III describes the proposed circuit topology with a focus on the pulse shaper and section IV gives the implementation and measurement results. Finally, Section V draws the conclusions.

II. SAMPLING MIXER PRINCIPLE

Conventional voltage passive mixers, as described in [3], are usually driven by a sinusoidal LO waveform or a 50% duty cycle square wave. These mixers often provide a low conversion gain ($2/\pi$ maximum value) which degrades the receiver NF performances.

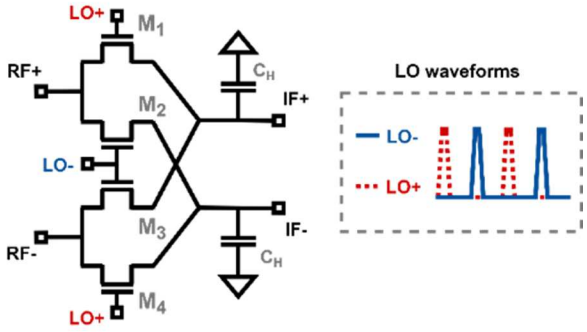

Figure 1: Sampling mixer principle

Passive mixer noise and gain performances can be enhanced by introducing a sampling operation. Applying a low duty cycle LO signal and voluntarily presenting a capacitive load at the IF outputs turns the mixer into a voltage sampler. This principle is proposed here in a double-balanced configuration (fig.1). Transistors are used as switches closed for a very short time to sample the input voltage. The hold capacitors C_H store the sampled values when all the switches are open. Considering that $M_{1,2,3,4}$ are conducting for a time $\tau_{ON} = D.T_{LO}$, the voltage conversion gain (G_{cv}) of a sampling mixer is calculated as:

$$\boldsymbol{G_{cv} = \frac{1}{2} sinc\left(\frac{f_{RF}}{f_{LO}}.D\right)\left(1 - e^{-j\pi\frac{f_{RF}}{f_{LO}}}\right)} \qquad (1)$$

According to (1), G_{cv} increases when D gets lower and tends toward 1 as the duty cycle D tends to 0. As a result, using a sampling mixer rather than a conventional CMOS voltage passive mixer allows to break the $2/\pi$ conversion gain limitation [3] to ideally reach the value of 1. This property of the sampling mixer increases the gain of the front-end before the baseband amplification. It will result in lowering the baseband amplification noise contribution thus improving the overall receiver NF.

Another strength of the sampling mixer is the linearity that depends on the transistors switching time [4]. When driven by

a LO signal with sharp rising and falling edges, these mixers are highly linear.

Benefits of sampling mixers have already been demonstrated around a few GHz and more recently at higher frequencies in [2]. The frequency performance of latest nm-scaled CMOS technological nodes let the sampling mixer appear as a possible option at 77 GHz. However, the 77 GHz low duty cycle LO signal generation is critical. Therefore, next section deals with a new 77 GHz pulse shaper and its implementation into a sampling mixer.

III. Circuit Description

The biggest challenge in implementing a 77 GHz sampling mixer is the low duty cycle LO signal shaping. A proper low duty cycle square wave requires many harmonics that cannot be generated or managed at such high frequencies because of too low transistors f_t and parasitic elements. Fortunately, a low duty cycle D and a sharp on/off transition can be obtained even if LO signal is not perfectly square. As demonstrated later in this paper, it is possible to generate 77 GHz waveforms able to drive the mixer close to the ideal sampling mode.

The conventional way to generate a pulsed waveform is to use logical gates but they exhibit a too poor mm-wave gain to reach the required harmonics amplitudes on the mixing transistors gate. An interesting solution is to use passive non-linear devices with very high cut-off frequencies to create these harmonics. The concept of Non-Linear Transmission Line (NLTL) based on varactors to turn a sine wave into a pulsed periodic LO signal illustrates this idea [5].

However, for a proper 77 GHz pulse shaping, the NLTL exhibits quite large length and a lower input impedance limiting the LO voltage swing and making an extra amplifying stage necessary. To overcome this limitation, a new pulse shaper architecture, inspired from NLTL, is presented in fig.2 (a).

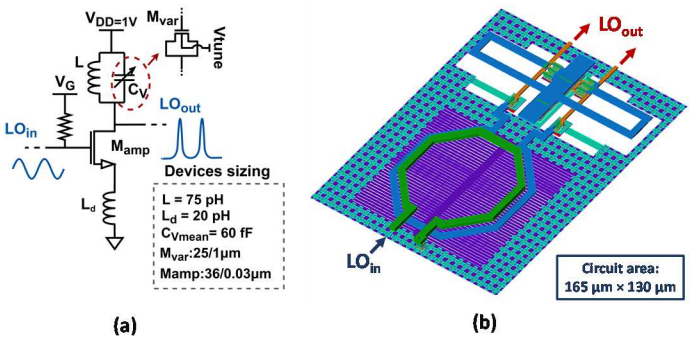

Figure 2: (a) Pulse shaper principle (b) Balanced pulse shaper layout

From this circuit the input sinus is amplified and turned into a pulsed voltage waveform at the same time. The common-source transistor brings the linear amplification of the LO input signal while the pulse shaping comes from the LC_v resonator. The impedance of the resonator is quickly varying according to C_v capacitance swing driven by the LO_{out} voltage amplitude. This impedance swing makes LO_{out} phase and magnitude alternatively increase and decrease over the LO period to create the pulsed waveform of the output signal LO_{out}. To have a sharp C_v(V) curve, variable capacitance is implemented with a transistor, using FDSOI body bias capabilities to tune the threshold voltage for optimum performance. To illustrate the behaviour of the circuit, a transient simulation of the standalone pulse shaper is presented in fig.3. All layout parasitic elements have been taken into account using momentum or PLS extracts. The displayed output voltage waveforms are obtained from an input LO power of 0 dBm and different varactors tuning voltages (V_{tune}) at 77 GHz. With the devices size presented in fig.2.a and $V_{tune} = 3\ V$, the pulse shaper generates a 1.4 V_{p-p} pulsed LO waveform with a duty cycle D_{LO} of 33%. This value appears to be the best performance that can be achieved because of limitations introduced by layout parasitics at 77 GHz. As reported in Table 1, this LO pulsed waveform improves mixer performances compared to a sine wave.

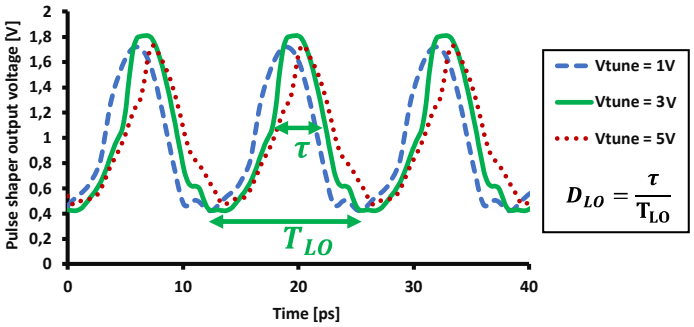

Figure 3: Pulse shaper output waveforms for different V_{tune}

To ensure the reliability of the pulse shaper even if output voltage reaches 1.8V (fig.3), V_{DS} and V_{GS} voltages have been monitored. As the V_{GS} is low (no current) when V_{DS} is high, the transistor is not subject to high hot carrier injection and stays inside its safe operating area.

This pulse shaper is very compact and much easier to drive than a NLTL, making this topology well suited to nm-scaled CMOS designs. The fig.2 (b) shows the layout of the balanced pulse shaper implemented with an input passive balun.

The second key point is the mixing transistor sizing which is essential to get a good noise/linearity trade-off. To get the best linearity from the sampling mixer, sharp LO pulse rising and falling edges are needed. However mixing transistors present a capacitive load to the output of the pulse shaper. This load tends to soften the LO pulse edges by presenting a low impedance at high frequencies. Small width transistors help keeping sharp LO edges, but on the other hand, increasing the width helps to reach a low NF, since the ON-state resistor r_{ON} of transistors is lowered. The resulting trade-off for the mixing transistors W/L ratio is 15 µm / 30 nm. The chosen C_H value is set to 300 fF. It is high enough to properly store the sampled value without limiting the circuit bandwidth.

Finally, to assess the sampling benefits, simulations with the same mixer driven with either a sinusoidal or a pulsed LO waveform coming from the pulse shaper (both with the same magnitude) have been performed.

The results of an harmonic-balance simulation performed at a f_{RF} and a f_{LO} of 77.02 GHz and 77 GHz, respectively, are reported in table 1. A global layout modelling using momentum and a PLS extract is included. Table 1 reports the simulated

voltage conversion gain, ICP1dB and Single Side Band (SSB) NF (NF_{SSB}) for both LO waveforms. This table shows that all the main characteristics of the mixer are improved when the sampling operation is enabled by using the LO pulse shaper and the hold capacitor C_H.

Table 1: Sampling and conventional passive mixers simulated performances

	LO Waveform	G_{cv} [dB]	ICP1dB [dBm]	NF_{SSB} [dB]
Passive sampling mixer	Pulsed	-1	+7.8	9.5
Conventional passive mixer	Sinusoidal	-4	+5.2	10.8

The voltage conversion gain G_{cv} of -1 dB is in good agreement with (1). The input-referred compression point is improved thanks to the sharper rise and fall times of the LO signal, and the NF using a 50 Ω RF source benefits from the lower LO duty cycle. The next section presents the implementation and the measurement results of the sampling mixer.

IV. Implementation and Measurement Results

The 77 GHz sampling mixer has been designed in a 28-nm FD-SOI CMOS process by STMicroelectronics. The whole mixer architecture is depicted in fig.4.a. A picture of the manufactured chip is given in Fig.4.b. The circuit area is 0.83 mm × 0.68 mm.

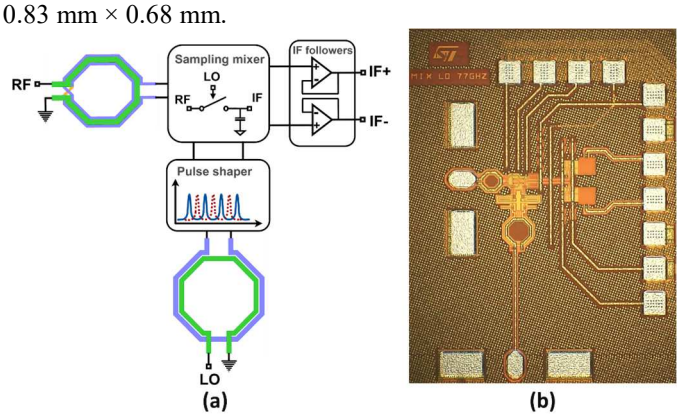

Figure 4: (a) RF mixer block diagram (b) manufactured chip

As differential 77 GHz signal synthesizers are not available, passive baluns have been added on-chip to feed the balanced RF and LO inputs. On the LO access, the balun is sized to optimize impedance matching. At IF frequencies, the mixer acts as a low-pass $1/g_c.C_H$ network where g_c is the mean channel conductance of transistors $M_{1,2,3,4}$ over the LO period. Because of the passive mixer transparency regarding impedances, this network results in a high RF input impedance ([6],[7]) around each odd LO harmonics ($n.f_{LO}$). An input passive balun with a 2:1 turn ratio is then implemented on the RF access to lower the mixer input impedance to 50Ω. This balun exhibits an 8.2 dB voltage gain as a consequence of its voltage transformation ratio.

Finally, Two Op-amps in follower configuration (0 dB gain) are implemented on the IF output to provide a high resistive impedance ($R_{IF} = 10$ kΩ) in parallel with C_H to ensure a good sampling.

Measurements of the RF voltage conversion gain (G_{c_v}) and the NF_{SSB} of the sampling mixer are reported in fig.5. They include the RF input balun performances. Fig.5.a and fig.5.b present G_{c_v} and NF_{SSB} , respectively, versus f_{RF} while f_{IF} is kept constant at 20 MHz. The G_{c_v} is measured between 7 dB and 8.5 dB and the NF_{SSB} between 10.5 dB and 13 dB in the f_{RF} range [76-81] GHz in good agreement with simulations. Fig.5.c depicts the RF voltage conversion gain with f_{RF} = 78.02 GHz and f_{LO} = 78 GHz when the input power is in the range [-20; 0] dBm. The extracted G_{c_v} and ICP1dB are respectively 7.5 dB and -1.5 dBm.

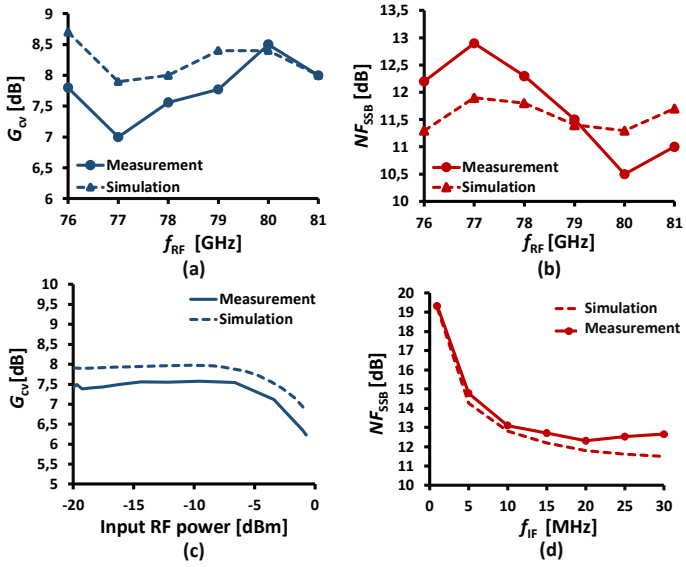

Figure 5: (a) G_{c_v} versus f_{RF}, (b) NF_{SSB} versus f_{RF} (c) G_{c_v} compression curve at f_{RF} = 78 GHz (d) NF_{SSB} at $f_{RF} = 78\ GHz$

The sampling mixer core performances are obtained by de-embedding the input RF balun from measurements. In these conditions, G_{c_v} is -0.7 dB and the 1 dB compression voltage V_{1dB} reaches 1.37 V_{pp} at the input of the mixer. Voltage is used to express the mixer compression point as it is more relevant for a high Z_{in} block and is equivalent to an ICP1dB of + 6.7 dBm in a 50Ω system.

Finally, fig.5.d shows the NF_{SSB} at $f_{LO} = 78\ GHz$ and an IF frequency range up to 30 MHz. Measurements of NF_{SSB} are performed using the cold source method. An increase of the NF_{SSB} under 20 MHz can be noticed due to the IF Op-amp $1/f$ noise. The measured value of NF_{SSB} is 12.3 dB at an IF frequency of 20 MHz. The Op-amp follower output stage has been characterized separately. The measured NF_{SSB} of the sampling mixer becomes equal to 9.1 dB after removing the noise contribution of the op-amp follower. The table 2 sums up the sampling mixer performances. These results show that the benefits of sampling mixers already demonstrated at lower frequencies [2] are also achievable in the W band with a 28-nm CMOS node.

Table 2: Sampling mixer measured performances

f_{LO} [GHz]	f_{IF} [MHz]	G_c [dB]	ICP1dB [dBm]	NF_{SSB} [dB]	P_{dc} [mW]
78	20	-0.7	+6.7	9.1	10 + 23*

* IF output follower consumption

As stand-alone passive mixers are not presented in the literature related to CMOS 77 GHz radar receivers, a meaningful comparison between this sampling mixer and other existing solutions is a bit difficult. The proposed sampling mixer has been implemented with a variation of the LNA presented in [8] in a 77 GHz front-end (LNA + mixer). As a result, a proper comparison with the state of the art can be provided. The measured front-end performances are summarized and compared with other radar receivers in table 3.

Table 3: Front-end measured performances and comparison

	LNA + this work	**[1]**	**[9]**	**[10]**
Tech	**28-nm FD-SOI CMOS**	40 nm CMOS	65-nm CMOS	22-nm FD-SOI CMOS
G_{RX} **[dB]**	**10.8**	16	26.2	16
ICP1dB [dBm]	**-7.8**	-7.8	-8.5	-3.5
NF_{SSB} **[dB]**	**9.4**	8.7	15.3	12.8
V_{DD} **[V]**	**1**	1.8	1	0.8/1.8 (RF/IF)
P_{DC} **[mW]**	**20**	NA	78	NA

The receivers in [1], [9], [10] are among the best noise/linearity trade-off reported in the literature related to 77 GHz CMOS radar receivers. As the receiver linearity strongly depends on the LO voltage amplitude, the receiver in [1] relies on a significant voltage supply to benefit from a high linearity. Another strategy is used in [9] and [10] where the one-stage LNA results in a low front-end gain ensuring a high linearity on a low voltage supply. In [10] the low front-end gain is compensated by the IF transimpedance amplifier (TIA) gain without degrading the linearity by taking advantage of the high baseband voltage supply (1.8V vs 0.8V for RF blocks). This strategy allows [10] to reach the best ICP1dB of this comparison by degrading a little bit the NF_{SSB}.

The solution proposed in this work relies on a sampling mixer showing at the same time a high linearity with low conversion losses on a 1V voltage supply. The pulsed LO waveforms keep the transistors in their safe area without sacrificing the linearity, which is a major challenge considering the low breakdown voltages of nm-scaled CMOS processes. As a result, the proposed receiver has similar performance to [1] but with a lower supply voltage. Compared to [10] and [9], the use of a 2-stage LNA increases the front-end gain reducing the NF_{SSB}. This comparison shows that the receiver based on the proposed sampling mixer ranks with [1], [9], [10] among the best existing trade-offs between noise and linearity. By operating under a 1V supply, this front-end also exhibits a low power consumption. Therefore, this topology appears to be attractive to design an high-performance CMOS automotive radar receiver.

V. CONCLUSION

A new sampling mixer, operating at mm-wave frequencies, is proposed. The discussion puts forward that driving the mixer with a low duty cycle LO signal, in addition to a capacitive load, creates a sampling behavior improving the conversion gain and linearity when compared with 50% duty cycle driven mixer. Nevertheless, the generation of a low duty cycle signal at 77 GHz is a critical point. As a solution, this paper introduces an innovative 77 GHz pulse shaper able to turn the LO signal into a pulsed waveform. The implementation of the LO pulse shaper and a double-balanced passive mixer in a 28-nm FD-SOI CMOS technology validates this new sampling mixer topology combining a good conversion gain with a high linearity. According to these results, the proposed sampling mixer appears as a good candidate to satisfy automotive radars stringent requirements.

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