Micron-to-Submicron Cu electroplating in view of Agile-X LSI Chips Fabrication using Open Facility

Naonobu Shimamoto¹, Ayako Mizushima¹, David Bourrier², Etsuko Ota¹, Akio Higo¹, Hugues Granier², Atsutake Kosuge¹, Makoto Ikeda¹, Tadahiro Kuroda¹, Yoshiho Mita¹, c

¹Systems Design Lab. (d.lab), the University of Tokyo; 7-3-1 Hongo, Bunkyo-city, Tokyo, Japan
²LAAS-CNRS; 7, avenue du Colonel Roche BP 54200 31031 Toulouse cedex 4, France

Type of Contribution: no preference

Abstract:

The goal of the Agile-X project at UTokyo d.lab, supported by MEXT X-nics, Japan, is to produce custom logic LSI devices (real silicon) in a very short turn-around-time, ideally, in one week. To achieve the goal, d.lab deploys a “structuredASIC™” approach. As shown in Fig.1, the transistors and functional building blocks (such as MPU and SRAMs) are pre-fabricated by a mega-foundry, and only adding a couple of metal wiring layers completes an LSI device. The key process is a chip-scale “back end of the line (BEOL)” fabrication with Q-TAT in Takeda Super Clean Room (SCR), Univ. of Tokyo. Both subtractive (etching) process for wider aluminum wirings and additive (electroplating) process for narrower copper (Cu) wirings are under development. This presentation will mainly focus on Cu wiring process optimization thanks to EU-JP international engineers’ cooperation.

First, a dedicated test structure to electrically assess the process performance is designed. Cu BEOL is developed using maskless lithography and electroplating in our SCR. Maskless lithography, such as laser and electron-beam (EB) direct writing on resist film, is a suitable prototyping method in agile and flexible for ever-changing circuit designs. Sub-micron-size fabricated delicate Cu structures on SiO₂/Si substrate by a semi-additive process (SAP) was tested. Cu 50 nm / TiN 10 nm film was deposited on the substrate by magnetron sputtering as the seed layer for electroplating and barrier layer for Cu. Resist-Polymer films (SIPR3251, SR7790, ZEP520A, etc.), patterned by laser or EB writing, respectively, were used as masks for Cu electroplating. Figure 2 shows the close-up view of (a) micro- and (b) submicron scale Cu structure on the substrate.

Acknowledgement:

This work was supported by MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS) Grant Number JPJ011438.

*Presenting author: N. Shimamoto, cCorresponding author: Yoshiho Mita (mita@if.t.u-tokyo.ac.jp)